

Libero Over view and Design Flow







Libero Integrated Orchestra







Libero Design Flow







Software Install







Libero Software Feature

Function	Tool	Vendor	Libero Silver	Libero Gold	Libero Platinum	Libero Platinum PS	Libero Platinum PS Eval	Designer Gold	Designer Platinum	Designer Eval
Device Suppor	t									
300,000 Gates and smaller		Actel	+	+	+	+	+	•	*	*
All Actel Devices		Actel	ā	25	*	+	+	070	*	*
Features Provi	ided									
Project Manager	Libero Software	Actel	+	+	*	*	+	878		
Design Entry (HDL)	Libero Software	Actel	•	+	+	*	*	17.1	2	
Design Entry (Schematic)	ViewDraw AE ¹	Actel	•	+	+	+	+	17		-
Synthesis	Synplify Lite ² / Synplify AE	Synplicity	* 2	4 2	*	*	*	17		-
Simulation	Model <i>Sim</i> AE	Mentor Graphics		+	*	*	+	07.0		-
Physical Synthesis	PALACE	Magma		27	170	*	+	870		-
Test Bench Generator	WaveFormer Lite AE	SynaptiCAD	*	+	*	+	+	878	-	





License Request

	1	l. <u>http://register.actel.com/RegSerial.asp</u> 접속
Actel	Products & Sendoes: Saftware Resistration 2	2. Evaluation 신청시 <u>here</u> click
	Libero Designer and Palace Registration and Licensing	8. Products 선택(Libero Evaluation)
den all	4	Ⅰ. HDL 선택 및 C:∖ vol 과 synplify 의 hostid 입력
allenie ()	Click HERE to obtain a license for a HREE Likero, Designer, or Palace product.	=> Synplify hostid는 설치후 synplify를 실행하면
dan II	Please enter year Software ID number: (new parchases and returning visitors)	
	The Softwars ID number is located on the CD jacket. If you previously registered a free or purchased production this site your Software ID was included in this email that container your license file.	
	Acalineatation are Licensin Libero Platin Evaluation A 45-day license for Libero Platin generation. This product is availat node-locked.	um PB excluding programming file sie on PC platforms only and is
	Ottain FREE Litero DECers Libero Silver	mplete Libero Silver product which nd Na Please follow these steps to obtain your Libero IDE License
	Designer Evaluation A 45-day license for Designer Pla generation. Select one license ty Node-Locked O Floating	Select one HDL: VHDL Verilog Please take care to make an <u>accurate</u> selection of VHDL or Verilog here. If you choose incorrectly, your license will not work, and will have to be exchanged. This will cause delay in use of your Libero IDE software.
	Designer Gold A FREE 1 year license for the co which supports all Actel devices This product is available on PC pl	Enter your PC's hard-disk C drive Volume Serial Number: The Volume Serial Number is an 8 character hexadecimal number of the form xxxx-xxxx. To obtain your Volume Serial Number type the following at a DOS or Command Prompt: (Note: You must use the C drive hexadecimal number) C:> Vol C:
	Palace A 45-day license for Magnum Der Synthesis software. Select one in	Enter your Synplicity Host ID:
	Evaluation Onde-Locked OFloating	Start->Synplicity->Synplity. A dialog box will display a message that includes the line Example Your hostid is: 79C88961 Enter your hostID in the box provided above, then click the Cancel button in the dialog box to exit Synplify.
ibero V5.	2 SP1	Please Specify platform: Win XP Win NT4 Win 2000
Apr 2004 /er52		

<6>



License Setup

- 1. Email로 받은 license.dat를 actel install directory에 copy
- 2. Os가 win2000, XP 일경우 내컴퓨터 등록정보->고급->환경변수 변수 LM_LICENSE_FILE 값 C:\<INSTALL DIR>\license.dat 변수 SYNPLICITY_LICENSE_FILE 값 C:\<INSTALL DIR>\license.dat 위 두항목을 추가.
- 3. OS 가 WIN98인 경우. libero V50 이상에서는 win98을 지원하지 않으므로 win2000, winXP로 사용할것.





Design Entry







Demo Design Block Diagram



- 1. Pll_block : 40Mhz input을 20Mhz, 80Mhz 의 clock 생성
- 2. Count_block : 20Mhz의 clock으로 16bit counter
- 3. Piso_block : counter 의 output을 1bit serial로 출력
- 4. Top : 세개의 sub_block을 통합





Libero Project Manager

Design Explorer Window

• 디자인의 계층구조 표시:

- Design hierarchy: source design에 대한 계층구조 표시

- File Manager : design의 구성및 결과 file 관리창

HDL Editor Window

• Verilog와 VHDL93 text editor

Process Window

 Design을 위한 다른 tools로 연결

Log Window

• Software 연결상태및 메세지창







Create Project

Now Project Wizard New Project Wizard Start	 1. Libero IDE V5.2을 실행 메뉴에서 File - > New Project 실행 Project Name, Location, Family, HDL 지정 2. Software 선택 (synthesis, stimulus, simulation) 3. Design file 추가 (HDL, testbench, netlist) 4. Finish
Cal Select Tools Project jocation: C:WAcklprijWdemo Browsa # - Droj Andr Fies Eamily Project jocation: C:WAcklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WAcklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WacklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WacklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WacklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WacklprijWdemo Browsa # - Stroit Finish Eamily Project jocation: C:WacklprijWdemo Browsa # - Stroit HDL type: C:WacklprijWdemo Witzsend Help Mew Project Witzsend Select Integrated Tools Select the tools you want to use mith your newsproject C	Note : VHDL 과 Verilog와의 mixed design은 지원하지 않음. 한 개의 HDL과 Schematic은 가능
Start Start Select Texts Add Fles Firish Kiew Project With 5 to Now Project With 5 to Now Project With 5 to Now Project With Start S	Add Edit Add Edit Formulation Completing the New Project Wizard Add Formulation Completing the New Project Wizard Add Files Start Start Add Files New Project Start Back see copied to your new project Start Start Mew Project Start Start Back see copied to your new project Start Start Back Symbol Files (-1) Files (-1) Project Name: demo Project Name: Symphry 7.3.6 Stimulation: WholeSim 5.76*
Libero V5.2 SP1 Apr 2004 Ver52	HoL Files (+, whd) + whd) AC Tgen Macros (+, gen Implementation Files (+, Stimulus Files (+, whd)+, what Help Kent> Finish Cancel Kent> Cancel



Design Flow



< 단계별로 실행 가능한 기능을 보여줌>

- **1. Design Entry Tools**
 - => HDL Text Editor
 - => ACTgen Macro Builder
 - => Schematic View draw
- 2. Synthesis
- 3. Simulation
 - => Modelsim
 - => WaveFormer Lite
 - => Stimulus Editor
- 4. Place & Route
- 5. Programming
 - => Flash Pro
 - => Silicon Sculptor





Create Design – PLL Block



ليد ليد تساد	\sim	
MACROS	Feedback	Configuration
<u>%</u>	C Internal	i⊄ Static I⊂ Dynamic
Ð	Primary Clock	I" Bypass PLL
	Frequency (MHz)	[20.0000
Moltiplexor	Delay (ns)	0.00
0	Phase Shift (Degree ()	
FIR-filter	Secondary Clock	F Bypass PLL
	Input Frequency (MHz)	10.000
2)	Frequency (MHz)	60.0000
RAM	Delay (ns) 5	0.00
D. Receiver	Generate	Reset Help



- 1. Design Flow 에서 actgen 을 선택 => 선택후 name : pll_block 입력
- 2. 왼쪽 MACROS 메뉴에서 PLL 선택
- < Parameter Setting >
- 3. Input clock 40Mhz.
- 4. Primary clock output 20Mhz => Delay : 기본 250ps 단위로 - 4ns~8ns 지정가능 => Phase Shift : 90, 180, 270 위상 변환 가능
- 5. Secondary Clock output 80Mh => Delay : 기본 250ps 단위로 - 4ns~8ns 지정가능
- 6. Generate Pll_block.vhd file





Creat Design – Count Block



<mark>≪ Libero IDE - C:₩Actelprj₩demo₩</mark>	demo.prj - [cnt_block.vhd]
B 📽 🕼 D 📽 🖬 ½ 🖻 🛍 🕰	≃ M A \$\$ 3 3 1 8 7
Default Configuration PII_block (pII_block, vhd) Cnt_block (cnt_block, vhd) 3 Design Hierarchy File Manager	<pre>01 cnt_block.vhd 02 library ieee; 03 use ieee.std_logic_1164.all; 04 use ieee.std_logic_arith.all; 05 use ieee.std_logic_unsigned.all; 06 entity cnt_block is 07 port (count_en, reset, clk20 : in std_logic; 08 count : out std_logic_vector(15 downto 0)); 09 end cnt_block; 10 architecture behave of cnt_block is 11 signal tmp : std_logic_vector(15 downto 0); 12 begin 13 process(reset, clk20) 14 begin 15 lif reset = '0' then 16 tmp <= (others => '0'); 17 elsif clk20'event and clk20='1' then 18 if count_en = '1' then 19 tmp <= tmp + '1'; 20 end if; 21 end if; 21 end if; 21 end if; 22 library ieee; 33 use ieee.std_logic_arith.all; 34 use ieee.std_logic_arith.all; 35 use ieee.std_logic_arith.all; 36 use ieee.std_logic_arith.all; 37 use ieee.std_logic_arith.all; 38 use ieee.std_logic_arith.all; 39 use ieee.std_logic_arith.all; 40 use ieee.std_logic_arith.all; 41 use ieee.std_logic_arith.all; 42 use ieee.std_logic_arith.all; 43 use ieee.std_logic_arith.all; 44 use ieee.std_logic_arith.all; 44 use ieee.std_logic_arith.all; 45 use ieee.std_logic_arith.all; 46 use ieee.std_logic_arith.all; 47 use ieee.std_logic_arith.all; 48 use ieee.std_logic_arith.all; 49 use ieee.std_logic_arith.all; 40 use ieee.std_logic_arith.all; 40 use ieee.std_logic_arith.all; 40 use ieee.std_logic_arith.all; 41 use ieee.std_logic_arith.all; 42 use ieee.std_logic_arith.all; 43 use ieee.std_logic_arith.all; 44 use ieee.std_logic_arith.all; 44 use ieee.std_logic_arith.all; 45 use ieee.std_logic_arith.all; 46 use ieee.std_logic_arith.all; 47 use ieee.std_logic_arith.all; 48 use ieee.std_logic</pre>
	end process; count <= tmp; end behave; Editor Window Design Flow cnt_block, vhd
▲ → Output 〈 Errors 〉 Warnings 〉 Info / Ready	Ln 20, Col 20 VHDL PA

- 1. Design Flow 에서 HDL Editor 을 선택
 - => 선택후 name : cnt_block 입력
- 2. HDL Editor Window 에서 cnt_block

coding

3. 저장시 Design hierachy 에 cnt_block 추가됨

<기존 design import 방법> # File => import files.. 메뉴에서 기존의 Design file 을 import 가능





Creat Design – Count VHDL Design

```
-- cnt_block.vhd
library ieee;
   use ieee.std_logic_1164.all;
  use ieee.std_logic_arith.all;
   use ieee.std_logic_unsigned.all;
entity cnt_block is
  port (count_en, reset, clk20 : in std_logic;
       count : out std_logic_vector(15 downto 0));
end cnt_block;
architecture behave of cnt_block is
   signal tmp : std_logic_vector(15 downto 0);
begin
   process(reset, clk20)
   begin
     if reset = '0' then
        tmp <= (others => '0');
      elsif clk20'event and clk20='1' then
        if count_en = '1' then
           tmp <= tmp + '1';
        end if;
     end if:
   end process;
   count <= tmp;</pre>
end behave;
```

- 1. Library 선언구문
- 2. Entity 구문 cnt_block의 입출력 signal 선언구문



 Achitecture 구문
 16bit counter with count enable and asynchronous reset





Creat Design – Syntax check



- 1. Coding 한 design의 syntax check를 위해 File Manager 로 이동
- 2. HDL Files에서 원하는 vhdl 파일을 선택 우클릭을 이용하여 Check HDL file 을 선택
- 3. 아래 output 창에서 syntax check 결과 확인





Creat Design – PISO Block



FAM: PA DIE: UNSET PKG: UNSET



- 1. Design Flow 에서 actgen 을 선택 => 선택후 name : piso_block 입력 2. 왼쪽 MACROS 메뉴에서 Register 선택
- < Parameter Setting >
- 3. Register의 종류선택 => Shift Register
- 4. Variations => Parallel input to serial output register
- 5. 추가적인 옵션 선택

=> Clear, Enable, Load, Clock 속성 명시

6. Generate Pll block.vhd file



Ready

MACROS

%

D

D

07

PLL PLL





Creat Design – TOP BLOCK



Delault Configuration Inp (top, vhd) I	<pre>Di</pre>
---	---------------

- 1. Design Flow 에서 HDL Editor 을 선택 => 선택후 name : top 입력
- 2. HDL Editor Window 에서 top design coding
- 3. 저장시 Design hierachy 에 top design 추가됨

<기존 design import 방법> #File => import files.. 메뉴에서 기존의 Design file 을 import 가능 #Note : design 의 상하 관계를 인식하여 자동으로 계층구조 표시됨







Creat Design – Top VHDL Design

-- top.vhd

library ieee; use ieee.std_logic_1164.all; use ieee.std_logic_arith.all; use ieee.std_logic_unsigned.all;

entity top is

end top;

architecture behave of top is component pll_block is port(GLB,GLA,LOCK : out std_logic; CLK : in std_logic); end component; component cnt block is port (count_en, reset, clk20 : in std_logic; count : out std_logic_vector(15 downto 0)); end component; component piso_block is port(Data : in std_logic_vector(15 downto 0); Enable, Shiften, Shiftin, Aclr, Clock : in std_logic; Shiftout : out std_logic) ; end component; signal tmp_cnt : std_logic_vector(15 downto 0); signal tmp_clk20, tmp_clk80 : std_logic; begin U1 : pll_block port map (tmp_clk20, tmp_clk80, open, clk40); U2 : cnt block port map (count_en, reset, tmp_clk20, tmp_cnt); U3 : piso_block port map (tmp_cnt, enable, shift_en, shift_in, reset, tmp_clk80, data_out); count <= tmp_cnt; end behave:

1. Library 선언구문

2. Entity 구문

Top design의 입출력 signal 선언구문



3. Architecture 구문

4. Component 선언구문 Sub block pll_block, cnt_block, piso_block 선언

5. Component port map 구문 Sub block간의 signal 연결

=> Top.vhd file도 syntax check를 통해 coding 검증을 함.





Synthesis - Synplify







Ver52





Synplify – Viewer



- 1. 합성된 schematic의 viewer
- 2. RTL view 는 source 를 이론적인 형태로 schematic으로 표시
- **3. Technology view** 는 actel library로 변환된 netlist를 schematic으로 표시 HDL로 설계된 design을 검토하기에 RTL view는 자주 사용됨.

<NOTE> Schematic viewer는 Synplicity 정품에서만 지원가능함. Actel OEM은 지원하지 않음







Layout – Designer Series







Designer Series – Compile 1



< Place & Route 과정>

1. Design Flow에서 Please & Route 선택 실행

* Designer s/w 에서의 Design Flow <Compile> device 선택 및 logic size 분석 <Layout> design place & route <Bitstream> program하기 위한 stp/bit file 생성 <Back- Annotate> Timing sim을 위한 파일 출력

* Sub menu <Netlist Viewer> gat level circuit 분석 <PinEditor> pin assign <ChipPlanner> layout 후 내부 cell의 위치정보 확인 및 변경 가능 <I/O Attribute Editor> I/O의 특성 부여 <Timer> design timing 정보 <SmartPower> power 소모량 측정

Libero V5.2 SP1 Apr 2004 Ver52

Post-Synthesis

Files

Place&Route

Contemporation

Place&Route

Designer



æ

Designer

Series



Designer Series – Compile

1. Compile 선택

2. Device (gate, package, speed, voltage) 설정











Designer Series – Compile



B Eile View Icels Op	tions	Help			_ # X
	0 😕	1 m	1=0	1	
r		Desig	n Flow ·		
Compile	•	► Lay	rout	Back-Ar	* ====
MultiVie NetlistViewer PinEditor	w Nav	iguto		Bilstr tribute	eam SmartPower
8 Incartar Summers			EOU	IOF	*
Part-Package: APA	075-PC	208			
Part-Package: APA Core Slot	075-PC	208	3072		
Part-Package: APA Core Slot RAM/FIF0	075-PC s: Slots:	206	3072 12		
Part-Package: APA Core Slot RAM/FIFO I/O Slots	075-PC s: Slots:	208	3072 12 158	(Globals: 4)	(PLLs: 2)
Part-Package: APA Core Slot RAM/FIFO I/O Slots	075-PC s: Slots: ; 128	206	3072 12 158 Usage:	(Globals: 4)	(PLLs: 2)
Part-Package: APA Core Slot RAM/FIFO I/O Slots Core Cells: RAM/FIFO Cells:	075-PC s: Slots: ;: 128 0	208	3072 12 158 Usage: Usage:	(Globals: 4) 4.2 percent 0.0 percent	(PLLs: 2)
Part-Package: APA Core Slot RAM/FIFO I/O Slots Core Cells: RAM/FIFO Cells: IDs:	075-PC s: Slots: ;: 128 0 23	208 > >	3072 12 158 Usage: Usage: Usage:	(Globals: 4) 4.2 percent 0.0 percent 14.7 percent	(PLLs: 2)
Part-Package: APA Core Slot RAM/FIFO I/O Slots Core Cells: RAM/FIFO Cells: IOs: PLLs:	075-PC s; Slots; ; 128 0 23 1		3072 12 158 Usage: Usage: Usage: Usage: Usage:	(Globals: 4) 4.2 percent 0.0 percent 14.7 percent 50.0 percent	(PLLs: 2)
Part-Package: AP/ Core Slot RAM/FIFO I/O Slots Core Cells: RAM/FIFO Cells: IOs: PLLs:	0075-PC s: Slots: : 128 0 23 1	206 	3072 12 158 Usage: Usage: Usage: Usage:	(Globals: 4) 4.2 percent 0.0 percent 14.7 percent 50.0 percent	(PLLs: 2)
Part-Package: AP/ Core Slot RAM/FIFO I/O Slots Core Cells: RAM/FIFO Cells: IOs: PLLs:	075-PC s: Slots: : 128 0 23 1 smings)	208 > > >	3072 12 158 Usage: Usage: Usage: Usage:	(Globals: 4) 4.2 percent 0.0 percent 14.7 percent 50.0 percent	(PLLs: 2)

1. Compile 완료시 device에 사용량 체크

Core Cells : 순수 사용할 수 있는 gate RAM/FIFO Cells : Memory block에 대한 사용량 IOs : 사용된 I/O 수 PLLs : 사용된 PLL 개수

- <추가적인 check point>
- # global resources : 네개의 external global 사용된 signal
- # 외부 GL pin에 할당을 하여도 내부적으로 사용된 fanout 에 의해서 global 지정은 다르게 나타날수 있음.





Designer Series – PinEdit



	\bigcirc		
A strategy and str	Dis Editor	w Navigator	UO Attribute
THE REAL PROPERTY OF	- nicouor	Comparation of	Editor

MultiView Navigator I File Edit View Lo	top +1 - [PinEditor] oic Backage Tools	Window Help	
8 8 9 9 1 N 8	44900		284
<u></u>			
D clk40			
- den countil	GND	21	
Aca contico			
CE count(4)	count(0)	2 (N.11)	
- CE count(5)			
- 00 count(6) - 00 count(7)	count(1)	3 (N,10)	
Count(8)	count(2)	4 (N 8)	
- CE count(100	cours(z)	4 (14,0)	
 Count(11) Count(12) 	count(3)	5 (N.6)	
CE count(13)			
- CEI count(14) - CEI count(15)		6 (N,3)	
Count_en			
D enable		7 (W,33)	
- III reset		9 (W 30)	
D shit.in		0 (00,00)	
	GND	9	
Z			
	<	40.48(.94)	2
	× · · · ∧ Output / Erro	is), warnings), Info), Find 1 /	
dy		Top View FAM: pa DIE: APAB	75 PACKAGE: 100 TOFP



<pin file="" 줄력=""></pin>	file->export->constraint files->gcf 줄뎍
<pin file="" 입력=""></pin>	file- >import source file- >add 후 gcf 입력





Designer Series – Layout





Libero V5.2 SP1 Apr 2004 Ver52

1. Layout 선택

2. Layout options

<Timing- Driven> constraint file(gcf)에 명시된 조건에 따라 layout을 실행함. <Run Place> place를 재실행 <Incrementally> 기존의 place 된 정보를 유지 <Lock Existing Placement (fix)> 고정시킨 cell에 대해서 유지

<**Run Route> route**를 재실행 <**Incrementally>** 기존의 **route** 된 정보를 유지

 <Use Multiple Passes> layout 시 시작 시점(Seed)을 다르게 하여 전혀 다른 layout 결과를 가져와 성능이 좋게 나온 결과를 채택함.
 => layout의 횟수를 지정
 => specific clock에 성능향상을 하기 위한 clock 지정

2. Ok







Designer Series – ChipPlanner





Libero V5.2 SP1 Apr 2004 Ver52

- 1. ChipPlanner 열기
- Memory block
 APA 075/150 : 위에만 Memory 위치
 APA 300이상 : 위 아래 두곳에 Memory 위치
- 3. Core cell(tiles)
- 4. Core cell의 내부 구조

block 단위로 location 위치 지정 가능





Æ

Designer Series



Designer Series – I/O attribute



NetlistViewer	MultiVie	w Navigator	I/O Attribute
- N BUISTY LOWER	rnzauor	Corperancer	Editor

MultiView Navigator [top] - [1/O Attribute Editor]						
8 8 2 2 4 8 K	《《四日	(9) 5 (2	20	=		
네티	Port Name	Macro Cell	I in # L	ocked	Output Load	
E O Ports	1 cik40	ADLIB:0033	16 -	2	Contraction of the local distances	
	2 coun#0)	ADLIB:OB33PH	93		35	
OD/Anune 🚥	3 count(1)	ADLIB:OB33PH	85		35	
	4 coun#2)	ADLIB:0833PH	84		35	
Country Country	5 count(3)	ADLIB:OB33PH	34		35	
Count 20	6 count(4)	ADLIB:OB33PH	35		35	
Colonia Sy	7 coun#5)	ADLIB:0833PH	33		35	
COUNK 4J	8 coun#6)	ADLIB:0833PH	32	-	35	
COUN(5)	9 count(7)	ADLIB:OB33PH	31		35	
- COUN#(6)	10 count(8)	ADLIB:OB33PH	29		35	
- Count 7)	11 count(9)	ADLIB:0833PH	69	-	35	
- Count(80	12 count(10)	ADLIB:OB33PH	92	-	35	
- 💶 ciaun#(9)	13 count(11)	ADLIB:OB33PH	18		35	
	14 count(12)	ADLIB: OB33PH	91		35	
- Count(11)	15 count(13)	ADLIB:0833PH	10		35	
- Count(12)	16 coun#14)	ADLIB:OB33PH	90		35	
- COUN# 130	17 count(15)	ADLIB:OB33PH	11		35	
- count(14)	18 count_en	ADLIB:8833	8		and the second second	
munh(15)	19 data_out	ADLIB:OB33PH	66		35	
	20 enable	ADLIB: IB33	59		1	
and data and	21 reset	ADLIB B33_GL1_4/IOTILE	60	7		
a data_bdt	22 shift_en	ADLIB B33_GL1_4/IOTILE	65	7		
1. 1. 0. 20. 10.	23 shift_in	ADLIB:833	58	-		
× X	Encrs ∧ Errors	λ, Warnings λ, Infoλ, Pind row 1, col 3 (FAM:pa (D)	1 / E: APAD	5 PAC	KAGE: 100 TOFP	

- 1. I/O attribute editor 선택
- 2. IO 별 사용 macro cell 표시
- 3. Pin # 지정 가능





Designer Series – Timer





6 top - Timer

Eile Edit View Tool Help

御御師十三一町にの御聞王堂

- 1. Layout 후 timer 선택
- 2. Select Clock => design 에 사용된 모든 clock 표시 timming 분석이 필요한 clock 선택
- 3. 선택된 clock에 대해서 최대 performance 표시
- 4. 요구 clock 성능 지정 가능



- 5. Paths 선택하여 timing
 - 분석 가능
- => 각각의 path 별로 timing 분석
- 1) input register
- 2) register register
- 3) register output
- 4) input output







Designer Series – Bitstream



ile <u>t</u> ype:	Bitstream
FlashLock • <u>N</u> o locking (off)	ISTAPL
C Use <u>keyed lock</u> Security key:	(Max length is 20 hex chars.)
C Use <u>p</u> ermanent l utput filename:	<u>G</u> enerate random key
	<u>B</u> rowse,

1. Bitstream icon 선택

2. File Type 선택

BitStream : silicon sculptor를 이용한 programming

STAPL : flash pro and flahs pro lite 를 이용한 programming

- 3. FlashLock 입력시 program, erase 불가
 - => Use Keyed Lock 선택시 device에 따라 19~65 자리의 hex 값지정가능
 - => Use permanent lock 선택시 random 값 지정
- 4. Filename 지정
- 5. Programming file 생성

Libero V5.2 SP1 Apr 2004 Ver52



æ

Designer Series

Designer Series – Backannotation



Extracted files directory Extracted file names: Extracted file names: Extracted file names: Extracted file names	ate		
Browse Extracted file names: top_ba Simulator language Yerilog Verilog VHDL93 Timing C Pre-Layout Status Current directory: C:WActelprjWdemoWdesigner Speed Temp. Voltage	es <u>d</u> irectory		_
Browse Extracted file names: top_ba Simulator language ✓ Yerilog ✓ VHDL93 Timing ✓ Pre-Layout Status Current directory: C:\#Actelprj\#demo\#designer Speed Temp. Voltage STD COM COM			
Extracted file names: top_ba Simulator language Verilog VHDL93 Timing C Pre-Layout Status Current directory: C:\#Actelprj\demo\designer Speed Temp. Voltage STD COM COM	Brov	/se	
top_ba SDF Simulator language C Verilog VHDL93 Post-Layout C Pre-Layout C Post-Layout Status Current directory: C:\#Actelprj\#demo\#designer Speed Temp. Voltage STD COM COM	names: 👩	Output format:	
Simulator language 4 Export additional files C Verilog VHDL93 Timing C Pre-Layout Status Current directory: C:WActelprjWdemoWdesigner Speed Temp, Voltage STD COM COM	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	SDF	Ŧ
Timing	nguage 4	Export additional file Kontensister Konten	s
Status Current directory: C:\#Actelprj\#demo\#designer Speed Temp. Voltage STD COM COM	avout	C Post-Lavout	
Current directory: C:\#Actelpri\#demo\#designer Speed Temp. Voltage STD COM COM			
C:WActelprjWdemoWdesigner Speed Temp. Voltage STD COM COM	ctory:		
Speed Temp. Voltage STD COM COM	j₩demo₩desig	ner	
STD COM COM	emn Voltage		1
	OM COM		
OK Cancel Holp		I Help	

Libero V5.2 SP1 Apr 2004 Ver52

- 1. Back- Annotate 선택
- 2. SDF(Standard Delay Format) 출력
- 3. Timing simulation을 위한 HDL 선택 Verilog / VHDL93
 - # libero에서는 VHDL87 은 사용하지 않음
- 4. Pin file / Netlist 출력 가능
- 5. 모든 과정이 끝난 후 저장
 - => .adb 파일로 저장되며 이 파일하나로 design의 모든 정보를 내포하고 있어 관리 요망.





ø

Designer Series



Stimulus – Wave Former Lite











Waveformer Lite – Clock Properties



<Clock 속성 수정> Clk40을 더블클릭 하면 Properties 창이 활성화 됨

Signal Properties		?		E
Name: clk40		Acti <u>v</u> e Lov	,	Na
Simulate Once Analog P	props	<u>G</u> rid Lines		Re
Drive C Simulate C	Watch	C Compar	e l	Fr
Boolean Equation: ex. (SIG1 a	nd SIG2) del	ay 5	-	Pe
	1700 N.			Pe 1
Clock: Jundocked	cett evel:	Ipos _		St
Clock Pro	percies		1	D
Clock Enable: Not Used	Advand	ed Register		Ri
Boolean Equation C Veri	log C VHE	ol C te		Fa
<u>₩</u> fm Eqn 8ns=Z (5=1 5	=0)*5 9=H 9	9=L 5=V 5	3	[r
Label Eqn Hex(Inc(0	,2,5))		•	P
Export Signal Directi	on: output		-	r
F Analog Display	Size	Ratio: 1		P
VHDL: std_logic 👻 v	erilog: reg		7	F
Radix: hex 💌 Bus	MSB: 0	LSB: 0		F
Falling Edge Sensitive	Rising Ed	ge Sensitive		
OK Cancel Appl	y Prev	Next	1	1

Edit Clock Paramete	rs	<u>?</u> [×	
Name: clk40	•		Clock name
Reference Clk: None		•	
Freq:	10. C K	Hz / US	Clock Frequency
Period: 1	00.	Hz (ns Hz (ns	
Period Formula: ex. 2*CLK0.	period		Clock Period
100.			
Starting Offset:	0.		Clock Offset
Duty Cycle %:	50.	50	
Rise Jitter (range):	0	0	Clock duty cycle
Fall Jitter (range):	0	0	
Mip L to H		0	
Max L to H:	0	0	
Min H to L:	0	0	
Max H to L:	0	0	
Rising Delay Correlation:	100	%	
Falling Delay Correlation:	100	%	
Rise to Fall Correlation:	100	%	
Invert (Starts Low)			
ок	Cancel	1	





Waveformer Lite – Edit Signal

▼ Bus MSB: 0

Cancel Apply Brev Next

☐ Falling Edge Sensitive ☐ Rising Edge Sensitive

LSB: 0

Radix: hex

OK





MaveFormer Lite - 10/agram - top_thench.bt/m-1

1. 일반 1 bit signal 의 입력은 high/low icon을 이용하여 입력 => 왼쪽그림에서 보면 현재 입력은 low로 선택되어 있으며 한번 low 입력을 주면 자동으로 high로 전환됨

S 2 8 3 5 5 4 4 4 4 5	
Add Clock Add Spacer Hold Text Peter	
82.00ns 0.000ps Ons 50ns 100ns	Signal Properties
reset	
	Name: reset
count_en	Simulate Once Analog Props Grid Lines
enable	C Drive C Simulate C Watch C Compa
shift_in	Boolean Equation: ex. (SIG1 and SIG2) delay 5
shift e	1
count[14-0]	Clock: Unclocked 💌 Edge/Level: pos
data out	Set: Not Used 🛒 Clear: Not Used
	Clock Enable: Not Used 💌 Advanced Registe
	Boolean Equation C Verilog C VHDL C TH
Left click and drag to move, double click to edit	Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V 5
	Label Eqn Hex(Inc(0,2,5))
e를 Click하여 move 가능	Export Signal Direction: output
·에 drag 하여 signal 값 변경가능	Analog Display Size Ratio: 1

Libero V5.2 SP1 Apr 2004 Ver52

2.Signal 속성으로 주는방법 => signal을 더블클릭하여 속성창을 open Wfm Eqn 을 이용

> 예) Ons=1 100ns=0 200ns=1 (50ns=1 50ns=0)*10





Waveformer Lite – Edit bus



signar Prope	rties	? 🛛
Name: reset		Active Low
Simulate Once	Analog Props	<u>G</u> rid Lines
• Drive C Sin Boolean Equation:	mulate 🔿 Wato ex. (SIG1 and SIG	h C Compare 2) delay 5
		*
Clock: Unclocked	d 💌 Edge/Le	vel; pos 💌
Set: Not Used	🝸 Clear:	Not Used 🛛 🔫
Clock Enable: No	ot Used 💌 🛛 A	idvanced Register
Boolean Equati	ion C Verilog	VHDL C TE
Wfm Eqn 8n	ns=Z (5=1 5=0)*5	9=H 9=L 5=V 5 👻
Label Eqn	Hex(Inc(0,2,5))	
Export Signal	Direction:	utput 👻
✓ Export Signa ✓ Analog Displa	Direction:	size Ratio: 1
Export Signa Analog Displa HDL: std_logic	Direction: C	Size Ratio: 1
Export Signa Analog Displa HDL: std_logic Radix: hex	Direction: Carrier Carr Verilog: Bus MSB:	Size Ratio: 1
Export Signa Analog Disple Analog D	I Direction: c	Size Ratio: 1 reg LSB: 0 ing Edge Sensitive

Libero V5.2 SP1 Apr 2004 Ver52 1. Bus signal에 입력을 주기 위한 icon 사용 => 왼쪽그림에서 TRI : Tri- state VAL: Valid Bus

2.Signal 속성으로 주는방법 => bus signal을 더블클릭하여 속성창을 open Wfm Eqn/Label Eqn 을 이용

예) wfm eqn => (100ns=V)*10 : 100ns 간격으로 10개의 bus 입력 Label eqn => Hex(Inc(0,2,10)) : 초기값 0, 증가치 2, 데이터 개수 10

> File("vectors.txt") => 파일에서 입력 Bin(RandInt(20,255)) => 랜덤값 입력



Ø

WaveFormer Lite



Waveformer Lite – Export files 1



1. 파일 저장은 btim 형식과 VHDL 형식으로 두가지 모두 출력 save as => Timing Project => top_tbench.btim save as => Testbench VHDL=> top_tbench.vhd => VHDL Wait with Top Level TestBench 을 선택

& WaveFormer Lit	te - [Diagram - t	op_tbench.btim	±]					
🚡 <u>F</u> ile Import/E <u>x</u>	port <u>E</u> dit <u>B</u> us	Parameter <u>L</u> ibs	<u>R</u> eport	<u>V</u> iew ()ptions	<u>W</u> indow	<u>H</u> elp	_ 8 ×
🗲 🛛 🗿 🖣 🖨								
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample Hold Text Marker	ніўн 🚾 тяі	VAL INVal →⊂ ⊃∞	뱃비 씻년	HEX	Q + Q F Q - Q F	2	
942.0ns 406.0ns	Ons	1500ns	1.0us	1 - 31 - 33	1.5us	,	2.0	us , ,
reset							8	^
clk40								
count_en								
enable	Л							
shift_in								
shift_en								
count[15:0]	45.2	502				25		
data_out								
								(778)
< >	<							>
				Sim	ulation In	active	INS	i O Coli





Waveformer Lite – Export files 2



Libero V5.2 SP1 Apr 2004 Ver52



<40>

WaveFormer Lite



Simulation - Modelsim







Libero Options – Simulation



🕏 Libero IDE - C:\Actelprj\demo\demo.prj - [Design Flow]				
🥱 <u>F</u> ile <u>E</u> dit <u>V</u> iew <u>P</u> rocese	Options Window Help			
	Project <u>S</u> ettings			
	Profile			
	Package Files Organization			
I E Project Design Files				

- 1. LiberoIDE 에서 options=>project settings 선택 => Simulation 선택
- 2. Simulation end time 설정
- 3. Simulation type 설정 MIN : best case sim
 - TYP : typical case sim
 - MAX : worst case sim
- 4. Resolution : simulation sampling time 설정 정확한 simulation 결과를 얻기 위해서는 ps 단위로 설정

Options Family Simulation Programming			2
✓ Use automatic Do file User defined Automatic Do file content ✓ ✓ Compile package files ✓ ✓ Include Do file wave.do Testbench entity name: ✓ Top level instance name in the testbend Ype: ○ Min ○ Typ ⓒ Max Vsim additional	1 Do file:	Simulation 1000ns stbench op>_0 solution: 1ps	run
			Default
	확인	취소	도움말





ModelSim – Select Stimulus



Default Config	Den HDL file Check HDL file Create Symbol	Desi
	S ynthesize	P
	Create Stimulus Open Stimulus Select Stimulus	;
	Bur Pre-Synthesis Simulation from Post-Synthesis Simulation Run Post-Layout Simulation	on .
	Run Silicon Sculptar Run FlashPro	
	Properties	
Design Hierarchy	Ele Manager	

- 1. Modelsim Simulator 열기
- 2. 여러 개의 stimulus 가 있을 경우 한 개를 선택
- 3. ModelSim 이 열리면서 자동적으로 compile, load design, simulation 실행



Run Pre_Synthesis Simulation : Function simulation Run Post_Synthesis Simulation : Gate simulation Run Post_Layout Simulation : Timing simulation

*정확한 design의 검증을 위해서는 위 세 가지의 모든 경우에 대해서 simulation 결과가 일치해야 함.



ModelSim – Select Stimulus



ModelSim ACTEL 5 7b.	p1 - Custom Actel Version	
Eile Edit View Compil	le Simulate Iools Window Help	
	100 ns 114 114 114 114 114	
Workspace 📰 🗐		_
Instance Dec Instance Dec Instance Dec Instance timuskus_0 clima D- top_0 top[t Viables viab vial_primitives vial vial_fining vial texis texis texis Texis Timuskus_0 clima vial_minutes vial_primitives vial_fining vial Texis	# Loading _/presynfix.pll_blockt/def_arch) # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.prw[vld_ad] # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.gllccet(vla_ed) # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.gllccet(vla_ed) # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.gllcvia_ed) # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.gll(vla_ed) # Loading C /kadir/Liberol/52/Madel/win32accem/. /actel/vhdl/apa.gll(vla_ed)	دا
Now: 2 us Delta: 5	sim:/testbench	1

	VFT / d / d d b h h m m m H	10 17
Austberch/ck#0 1		NUNTUR
Astberch/count_m 1 Astberch/crable 0		
Z Asstandvihit in 0	ويستعد بتويير ويستعلن و	
Astbanch/count 0026		iener
0 teo_stablectured test		
11.42 March 1		
Monte II II The	500 at 1 ut 1500 at	218

Libero V5.2 SP1 Apr 2004 Ver52

ModelSim 이 열리면서 자동적으로 compile, load design, simulation 실행

<Note> macro file 관리

modelsim에서는 세가지 simulation 모두같은 run.do 의
macro를 생성하기 때문에 이름을 따로 지정하여 관리하는
것이 편리함.
예) func.do, gate.do, time.do

<macro file>

menu 에서 tools - > macro - > file 선택하여 실행 가능







ModelSim – macro file



Timing Simulation vlib postlayout vmap postlayout ./postlayout vcom - 93 - work postlayout ../designer/top_ba.vhd vcom - 93 - work postlayout ../stimulus/top_tbench.vhd vsim - t 1ps - sdfmax /top_0=../designer/top_ba.sdf postlayout.testbench add wave /testbench/* run 2000ns

Libero V5.2 SP1 Apr 2004 Ver52



ModelSim



ModelSim – wave









ModelSim – Internal Signal



<내부 signal을 보기위한 방법>
1. View - > Signals 과 Structure 창을open
2. Structure 창에서 sub-block으로 이동
3. Signals 창에서 원하는 signal 을 선택하여 add- >wave 를 한다.

<add 방법> selected signal : 선택된 signal 만 add selected in region : 선택된 block의 내부의 signal 만 add selected in design : top block의 이하의 모든 signal add



Libero V5.2 SP1 Apr 2004 Ver52



ModelSim



ModelSim – Save wave.do



File Edit View Compile 5	imulate Tools Window Help	land has
STAR ST SHOW	10 (5 14 15 15 16 17 16 17 17 17 17 17 17 17 17 17 17 17 17 17	
Wokapace		
Veronicipade Instance Design Unit De Instance Design Unit De Instance Ins	H Loading /persynth pins_block(del_ench) H Loading Cr/ools/Libero/%2/Model/him32accom/ /e H Loading Cr/ools/Libero/%2/Model/him32accom/ /e H Loading Cr/ools/Libero/%2/Model/him32accom/ /e H Loading Cr/ools/Libero/%2/Model/him32accom/ /e Weiw tachtre H structure view signatic L.signatic VSIM 42 rectart 4 VSIM 55 run 2 str	schel-Vrhälvppa musiäh(vhal_est) ushel-Vrhälvpa ditc[vhal_est] ushel-Vrhälvpa bitval_est] ushel-Vrhälvpa mv[vhal_est]
Library sin Files		
Now 2us Delta: 5	simi/testbench	
Elle Edit View Insert For S S S S I A A A A	nat Iaols Window 최근관 독명 역역역[[파티카]]	101 01 01 13-
File Edit View Insert For Company of the State of the St	mat Iools Windaw Art±rikisii@,@,@,@,priarian 	46 20 40 10
File Edit View Insert For Sector Academic View Insert For Academic View Insert For Academic View Insert Academic View Insert Ac	mət Iools Window A ± ± T K tol Q Q Q II I I I I I IIII I I I I I I I I	
File Edit View Insert For Sectors in the sectors of the sectors o	mat Iools Window Artsrik Bylesser Stratian	
File Edit View Insert For Sectors in the sectors of the sectors o	mat Iools Window A total i K tol i R R R II II II I I I I I I I I I I I I I I I	
File Edit View Insert For Sectors in the sectors of the sectors o		
File Edit View Insert For File Edit View Insert For Aestbench/reset Aestbench/ck40 Aestbench/count_en Aestbench/shitt_n Aestbench/shitt_en E- Aestbench/shitt_en E- Aestbench/count Aestbench/count Aestbench/count Aestbench/count Aestbench/count Aestbench/count Aestbench/count		
	mat Iools Windaw A ± ± [] []]]]]]]]]]]]]]]	
File Edit View Insert For Sector Content Aestbench/Count_en Aestbench/Shift_n Aestbench/Shift_n Aestbench/Count		
	mat Iools Window A ± ± T 1	
	mat Iools Window A t t I K B R R R I I I I I 1 1 1 1 1 1 1 1 1 1 1 1 1	

Libero V5.2 SP1 Apr 2004 Ver52 <Add 된 signal의 결과값은 나오지 않으므로 simulation을 다시 실행해야 됨>

1 Modelsim main windows에서 vsim #> restart –f vsim #> run 2 us

```
를 실행
```

- 2. Wave 창에서 결과 확인
- 3. Wave 창에서 wave.do로 저장하게 되면 다음에 이 추가된 signal이 자동으로 올라오게 됨
- **NOTE**> 저장된 wave.do를 자동 인식하기 위해서는 Libero의 options- >project settings.. - > simulation 에서 Include DO file을 check 시 자동으로 불려오게 됨.





Programming – Flash Pro / Silicon Sculptor







Flash Pro – programming



	(1)	
₽	Programming	Programming
STAPL File	FlashPro	Silicon Sculptor

	💩 Actel FlashPro	
2	File Help	
	File: C:\Actelprj\demo\designer\top.stp	
(3)	Action: PROGRAM	
	Device: Flash/Pro	
	Log Device Info	
	STAPL file loaded successfully	
	×	

Program 하기 위한 방법

- ⇒ Flash Pro를 이용한 방법
- 1. Design Flow에서 FlashPro 선택
- 2. File- > Connect..
 - => Computer와 FlashPro와 연결상태 확인 File- > Analyze chain
 - => board 상의 actel device를 확인

 - File- > Open Stapl File => Designer 에서 만든 .stp file load
- 3. Action 에서 PROGRAM 선택
- 4. Device- > 한 board 안에 2개이상의 device가 있을경우 program 할 device 선택
- 5. Execute icon 클릭
- => Program 완료 후 Pass, exit 0.





Flash Pro – programming



- # Flash Pro 를 이용한 다수의 device에 programming 순서
- 1. Flash Pro의 전원을 on
- 2. Target Board와 Flash Pro 의 케이블 연결
- 3. File- > connect를 선택, 해당 option check
- 4. File- > Analyze chain 선택
- 5. Device 와 Program file 을 선택
- 6. Program 실행
- 7. 완료 후, Flash Pro 케이블 분리
- 8. 다른 Target Board 와 연결
- 9. 위 4~8 항목을 반복



Silicon Sculptor – programming





SculptW V <u>F</u> ile <u>T</u> ools	4,40,0 11/04/2003
Quantity: 1	
BP-1600 De	mo Mode
<u>D</u> evice	Actel APA075-ISP Sher 1D654x8H
Data Pattern	top.bit CSUM=1227F5 04-22 2004 Buffer Size=1D654 bytes
Device <u>C</u> onfig	Set: 1 wide, 1 bank; Mode: Sets
Program ⊻erify ✓ Auto Sele ✓ Frase	Secure Erase
☑ Program	
Verify Tw	ice 🔽
Secure(K	EY_LOCK •
<u>E</u> XECUTE	STOP
File C:\Actelprj\de	emo\designer\top.bit loaded as PROASIC

Libero V5.2 SP1 Apr 2004 Ver52 # Program 하기 위한 방법

- ⇒ Silicon Sculptor를 이용한 방법
- 1. Design Flow에서 Silicon Sculptor 선택
- 2. Device > program 할 device 선택
- 3. Data Pattern > Designer 에서 만든 .bit 파일 open
- 4. Device config > 한 board 안에 2개이상의 device가 있을경우 program 할 device 선택
- 5. Auto Selection/Erase/Program/Verify Twice 선택
- 5. Execute icon 클릭
- => Program 완료 후 Pass, exit 0.
- => 장비가 제대로 연결되어있지 않으면 Demo Mode 로 나옴. 정상동작시 program할 adaptor의 명칭이 올라옴.





Schematic Design – View Draw









Libera - demo		a Di Xi
The Edit Yiew Bluess	Inols Window Holp	
	· · · · · · · · · · · · · · · · · · ·	
		1
Default Computation Top Default Computation Default Computation Default Computation Default Computation Default Computation	New	×
	File	04
Design Hierarchy File Maxoger Design Entry Utilities HDL Editor ViewDraw for Actel	FOR Insula ALTeen macro VHDL Entity VHDL Package File Stimulus Stimulus HDL File	Cancel Halp
Sunthesize		
🕑 💶 Synpility Synthesis	Name:	
- Simulation	Isourcobi	
Marker unter Life Samo Marker ModelSim Simulation Implement Designer Place-and-Ro Silicon Sculptor Silicon Explorer	aute	
nvaking Viewdraw he tutorial_sch project he demo project was aper	was closed. ned.	3
les-		<u> </u>
		the second se

1. New Schematic file 생성(new->Schematic)









- 1. Component 선택시 두가지 방법
 - i. Command line 에서 원하는 component 를 입력 => com and2
 - ii. Add component 에서 원하는 component 를 선택

















- Bus 연결은 bus icon을 이용하여 component 간의 pin을 연결한다.
 i. 단축키 를 이용할 수 있다.
- 2. Bus name은 Bus properties에 label에 name을 준다.
- 3. Index를 위하여 [7:0] 의형태를 갖는다.
- 4. 배열을 주기위해서 component properties에서 array option을 이용한다.

















- 1. Vhdl 로 구성된 top design을 schematic의 sub block으로 만들기 위해서 create symbol
- 2. Add component에서 top design을 import 하여 net를 연결한다.









- 0 ×

- 1. Vhdl top design과 schematic 과의
- 2. Add component에서 top design을 import 하여 net를 연결한다.



🕵 ViewDraw – [sch\sch_top]

