Actel FPGA Family

I&C MICROSYSTEMS / TERATECH Div.

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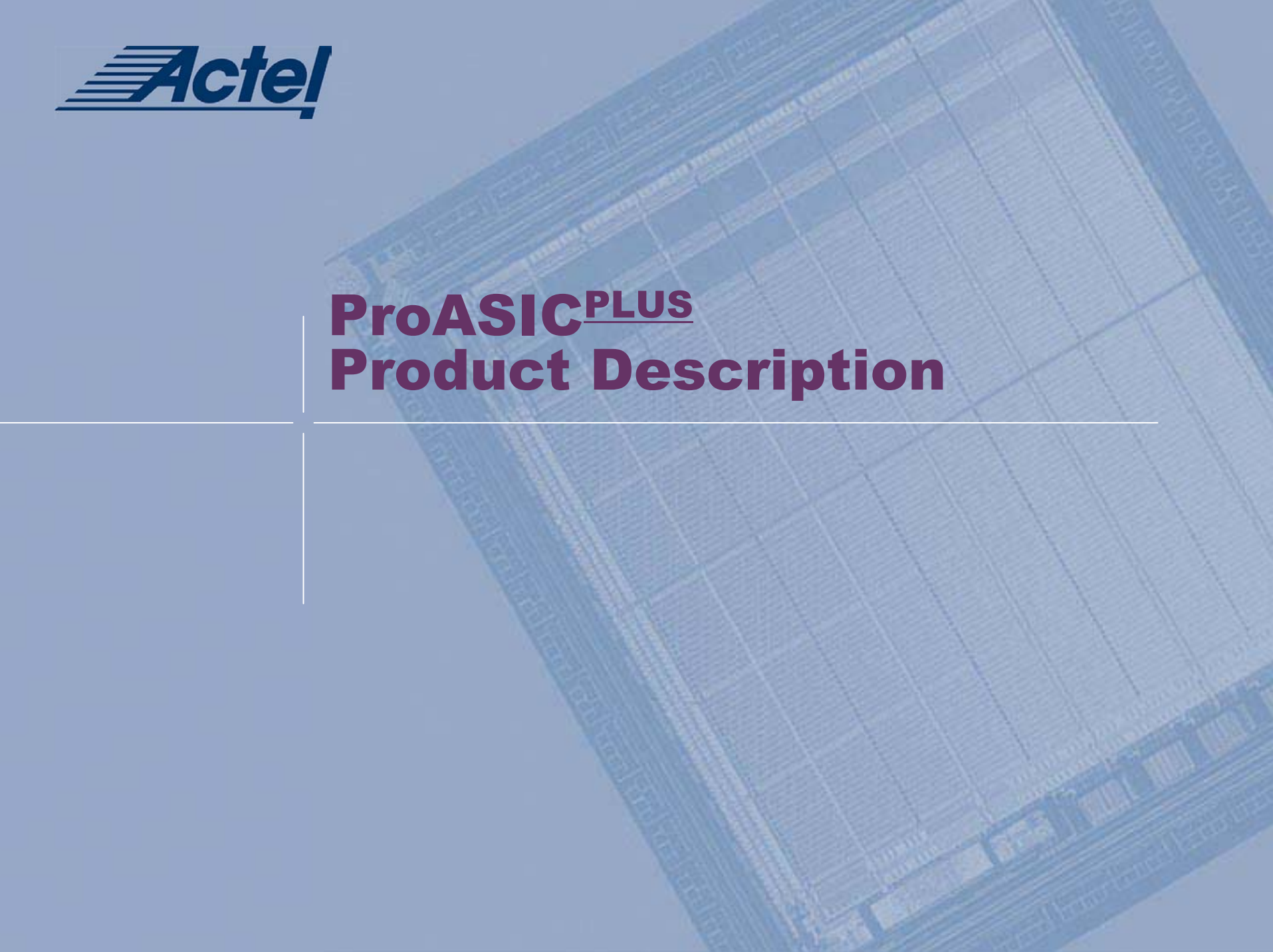


ProASIC PLUS
Product Description

What Is ProASIC?

0.25µ Flash-based programmable device

- Reprogrammable and non-volatile
- Live at power-up
- Cost effective, single-chip solution

Fine-grained architecture

- Predictable performance and high utilization
- Ideal for ASIC or FPGA design flows
- Designed for IP re-use
- 1/3 - 1/2 the power of LUT-based PLDs

Embedded memory/FIFO blocks

Design and IP security features

What Is ProASIC^{PLUS}?

0.22μ 4LM Flash-Based CMOS FPGA

Enhances system design capability

- Programmable logic up to 56K registers
- Large amount of configurable SRAM up to198kbits
- Key Analog functions (PLL and LVPECL)
- High performance IOs with 50 MHz PCI
- In system programming

Other High Value ProASIC^{PLUS} Attributes

- Re-programmable, single-chip, live at power-up
- Fine Grained Architecture for predictable performance
- Embedded FIFO Blocks with dedicated control logic

ProASIC A500K Family

	A500K050	A500K130	A500K180	A500K270
System Gates	98,000	287,000	369,000	473,000
Typical Gates	45,000	105,000	150,000	220,000
Max Registers	5,376	12,800	18,432	26,880
Embedded RAM bits	14K	46K	55K	65K
Embedded RAM Blocks (256x9)	6	20	24	28
Max User I/O	210	312	368	446

ProASIC^{PLUS} Family

	ProASIC^{PLUS}						
	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
ASIC Gates	20,000	40,000	80,000	100,000	150,000	200,000	300,000
Max Tiles (registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM bits	28K	36K	72K	108K	126K	144K	198K
Embedded RAM Blocks (256 x 9)	12	16	32	48	56	64	88
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	16	32	32	48	56	64	88
Max User I/O	158	242	290	344	454	562	712

ProASIC vs. ProASIC^{PLUS} Features

	ProASIC	ProASIC^{PLUS}
Family Members	4	7
PLL	NO	YES
LVPECL (Clock & Data)	NO	YES
PCI Support	33MHz	50MHz
Maximum Memory	63K bits	198K bits
Maximum User I/Os	440	712
Maximum System Gates	473,000	1,000,000
ISP	"YES" **	YES
System Performance "Normalized Level"		30% faster

* target is 500

**w / core power off

ProASIC^{PLUS} Product Overview

- More family members (7 added to existing four ProASIC members)
- Supports more complex designs
  - Larger devices
  - More routing resources
  - More memory
  - Faster user I/Os
- Improved system level performance
- PLLs for improved clock management
- True ISP support (JTAG, Processor, Daisy Chain)

ProASIC^{PLUS} is significantly improved in all areas from the original ProASIC product family

Additional ProASIC^{PLUS} Attributes

Analog clock conditioning functions

- 2 PLLs
- 1.5 to 240 MHz input and 6.0 to 240 MHz output frequency
- Multiply, Divide and Delay options
- Phase shifts of (90 ,180 ,270)
- Two high speed LVPECL differential pairs (Clock or Data inputs)

In System Programming

- MircoProcessor Interface
- Programming Header

High Value Design Security Lock

- User programmable key from 51 up to 263 bits

ProASIC PLUS Advantages

- ASIC-like tools and methodologies
- Improved in-system programming
- Maximum design security
- Flash-to-ASIC conversion program

ProASIC PLUS IP Support

Bus Interface

- PCI
  - 32 & 64 bit Master, Target, Master/Target Target + DMA, Arbiter
- PCMCIA, I2C, SPI, CAN, USB 1

Communications

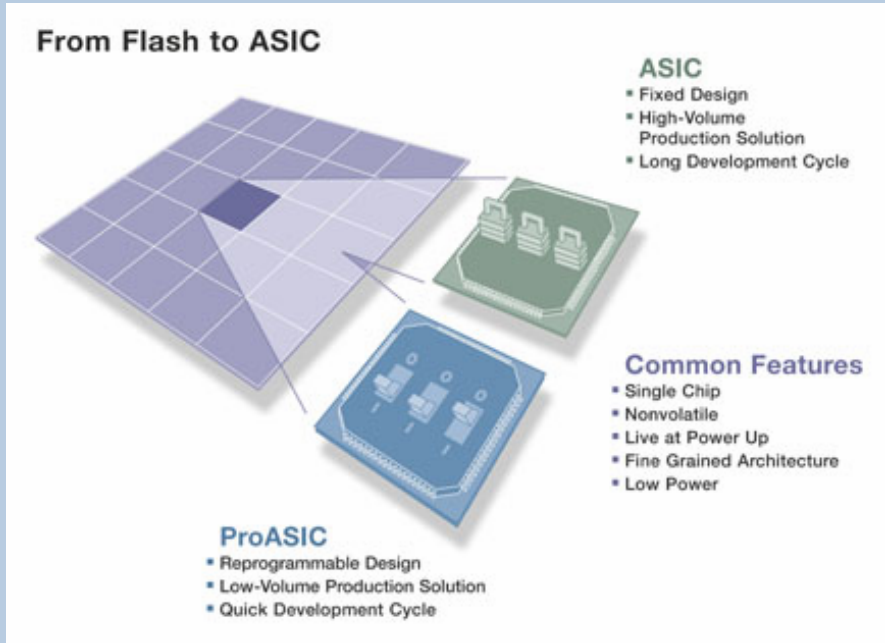
- UARTs – Generic & 16x50
- HDLC with FIFO
- 10/100 Ethernet MAC
- T1/E1 Framer
- FECs (Reed Solomon & Viterbi)
- Utopia 2 & 3

General Purpose

- Processors - 8051, 6809, 16 & 32 bit RISC
- Memory Controllers - SDRAM
- Encryption – AES, DES, Triple DES
- Multi-channel DMA
- Real-Time Clock

Flash-to-ASIC Conversion Program

- Actel certified ASIC partner, minimizes conversion risks
- ASICs fabricated by UMC, an Actel foundry partner
- Conversion facilitated by fine-grained architecture
- Supports all Actel flash FPGA products pin-for-pin
- Actel single point of contact throughout product life cycle
- Supports commercial and industrial temperatures

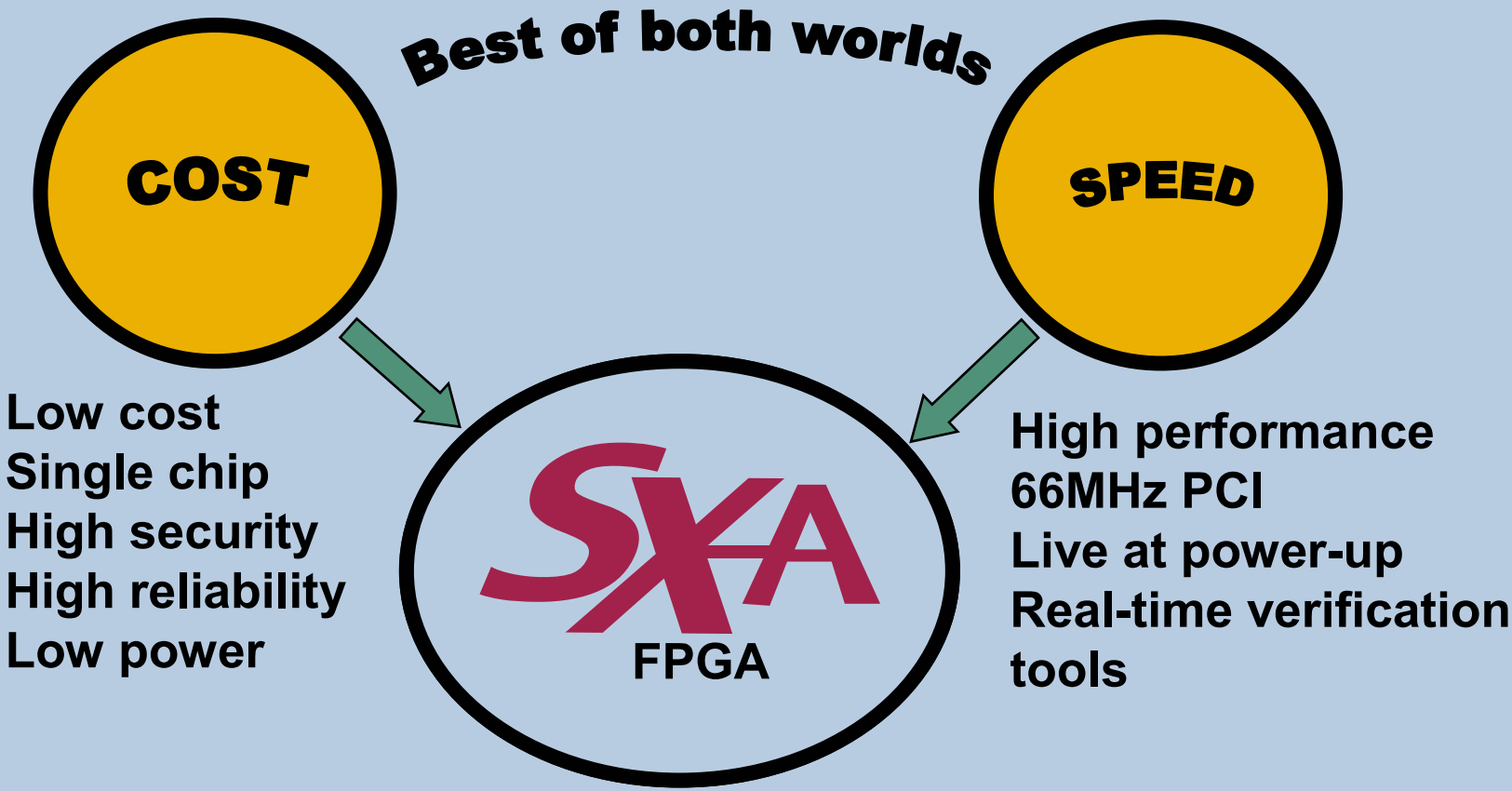


Flash Programmer

- Small form factor - 24 in^3
- Low cost
- Hardware features
  - Small 26-pin header
  - 20” ribbon cable
  - ECP Parallel port
- Software features
  - Win 95/98/NT/00 O/S
  - STAPL support
  - Daisy chain capability
  - Log file generation

Antifuse
Product Description

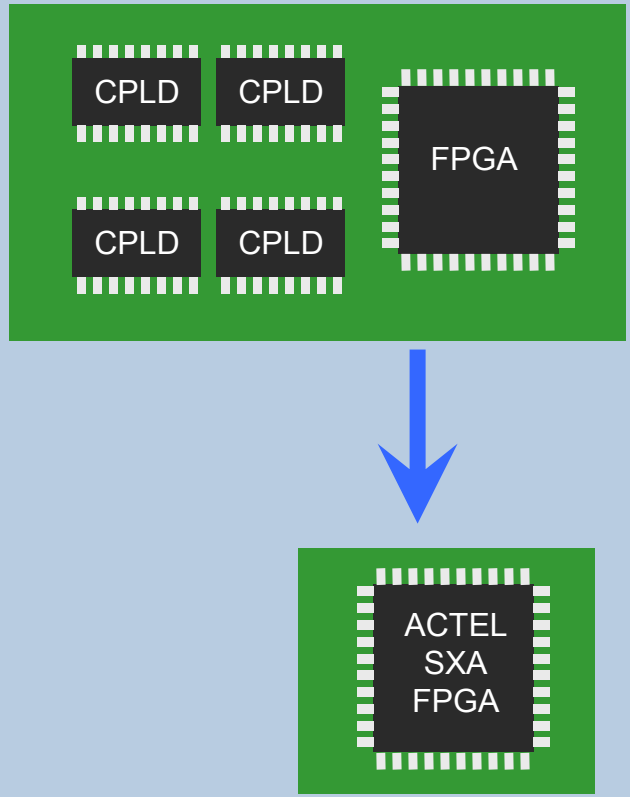
New Price/Performance FPGA Leader



SX-A / SX Benefits

Single-Chip Solution

- Live on power up
- Nonvolatile
- Lower cost and less board space than SRAM FPGA + boot PROM



Design Security

- Impossible to reverse engineer
- No boot-up bitstream to be intercepted

Trouble-Free Routing

- Maximum utilization of available resources

Pin Locking

- Allows any logic cell to route to any I/O
- Start PCB design ahead of FPGA design completion
- Maximum flexibility for faster time to market

Push-button HDL design flows familiar to CPLD and ASIC users

SX-A Family

	SX08A	SX16A	SX32A	SX72A
System Gates	12,000	24,000	48,000	108,000
Typical Gates	8,000	16,000	32,000	72,000
Logic Modules	768	1452	2880	6048
Dedicated Registers	256	528	1080	2016
Max User I/O	130	177	249	360

eX FPGA Benefits

Low Power

- Low Standby Current
- Sleep Mode (<100uA standby Icc)
- Selectable low slew on each output
- Extends battery life
- Enables higher reliability

High Performance for Speed Guard-band and Predictability

Versatility and Flexibility for system integration

- Hot-swapping support (no power-up/down sequence)
- Mixed-voltage support
  - 2.5V, 3.3V or 5.0V drive
  - 5V tolerant I/Os
- Boundary Scan Testing (IEEE 1149.1 “JTAG”)

Space-saving Chip-Scale Packages (0.8mm ball pitch BGA)

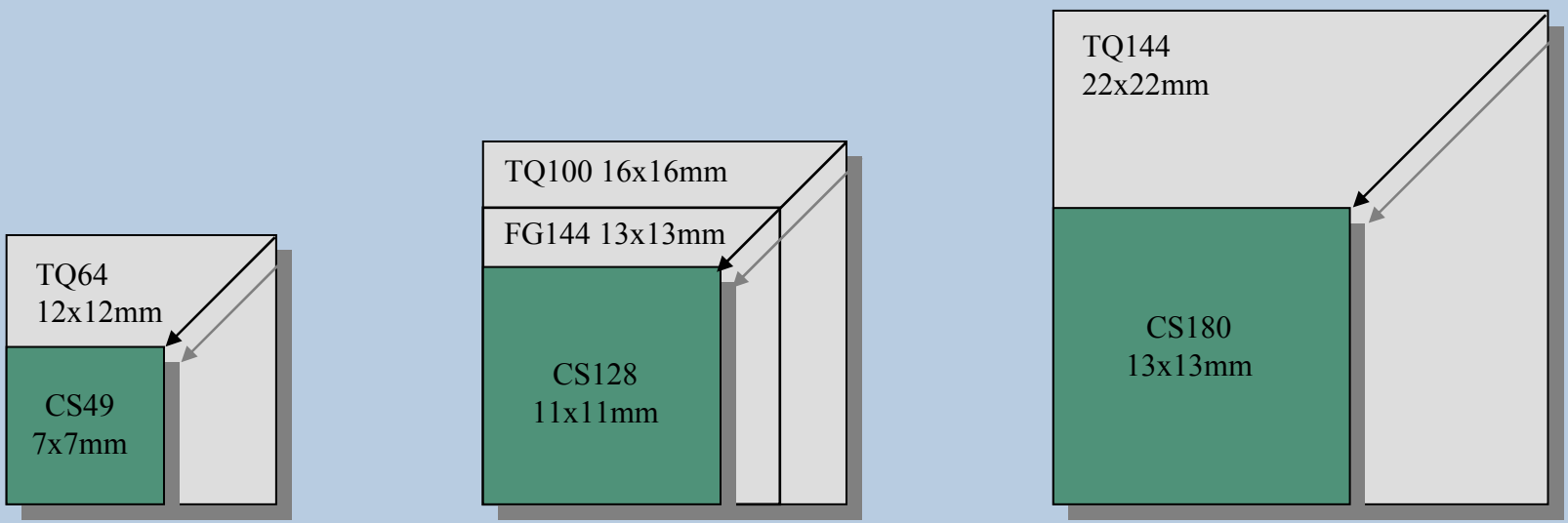
eX Family

	eX64	eX128	eX256
System Gates	3,000	6,000	12,000
Dedicated Registers	64	128	256
Combinatorial Cells	128	256	512
Max User I/O	81	97	130
Packages	TQ64 TQ100 CS49 CS128	TQ64 TQ100 CS49 CS128	TQ100 CS128 CS180
Speed Grades	-F, Std, -P	-F, Std, -P	-F, Std, -P

-F = 40% slower than Std
-P = 30% faster than Std

New Packaging

- *eX* Will Offer New Packages to Actel's Line up - the Chipscale
- ChipScale, Also Know As µBGAs, Are BGAs With .8mm Ball Pitch
- *eX* Will Offer the Following ChipScale Packages:



AX-Platform Overview

Technology

- 0.15 um 7 Layer Metal CMOS
- Amorphous M2M Antifuse

Architecture

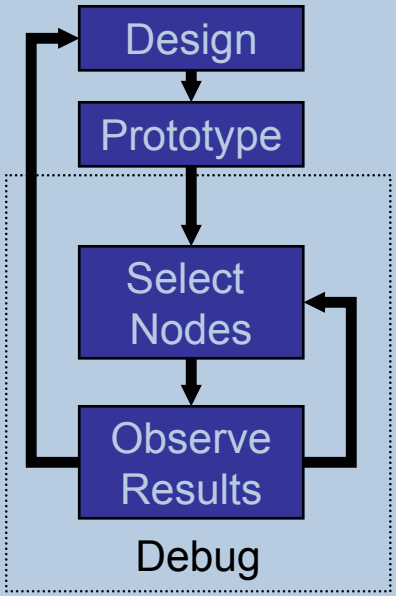
- SX-A Like - C cells & R Cells
  - Carry Chains - Faster Arithmetic
  - Enhanced chip-level routing
- Improved High-fanout Performance
  - Automatic Buffer Insertion
- 8 Segmentable Global Clocks
  - 4 HCLKs, 4 RCLKs
- Global Input/Output Enable, Clear and Preset
- Improved Programming Interface

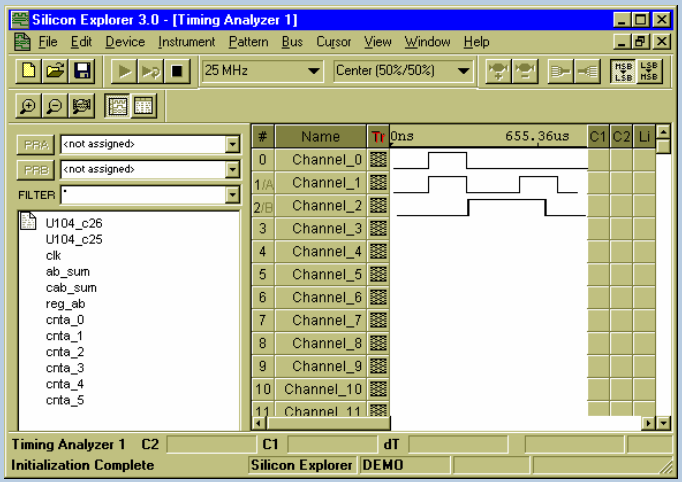
	AX125	AX250	AX500	AX1000	AX2000
System Gates	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Registers	672	1,408	2,688	6,048	10,752
Modules	2,016	4,224	8,064	18,144	32,256
RAM Bocks	4	12	16	36	64
I/O FIFOs	172	256	336	516	684
RAM (Bits)	29,440	71,680	95,232	198,912	338,688
PLL's	8	8	8	8	8
User I/O's	172	258	336	516	684
Packages	CS180	FG256	FG484	BG729	FG896
	FG256	FG484	FG676	FG896	FG1152

Silicon Explorer

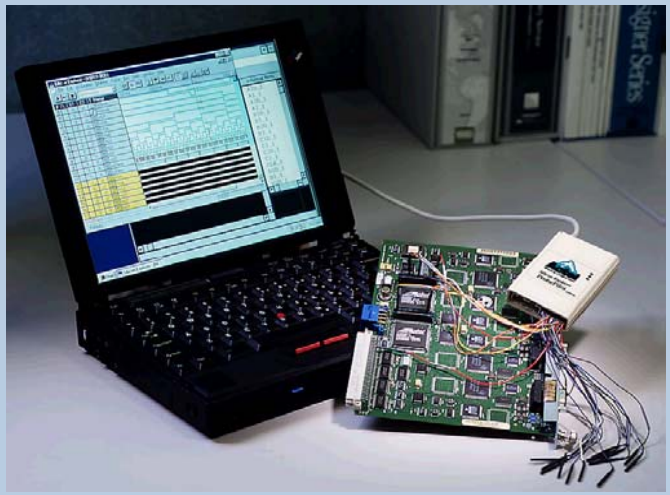
Debug your design in real time!

- Select internal nodes of the FPGA on the fly for viewing while device is running at FULL Speed!
- The only true real time debugging FPGA solution!
- Software delivered as part of the DeskTOP tools and Designer Series tools

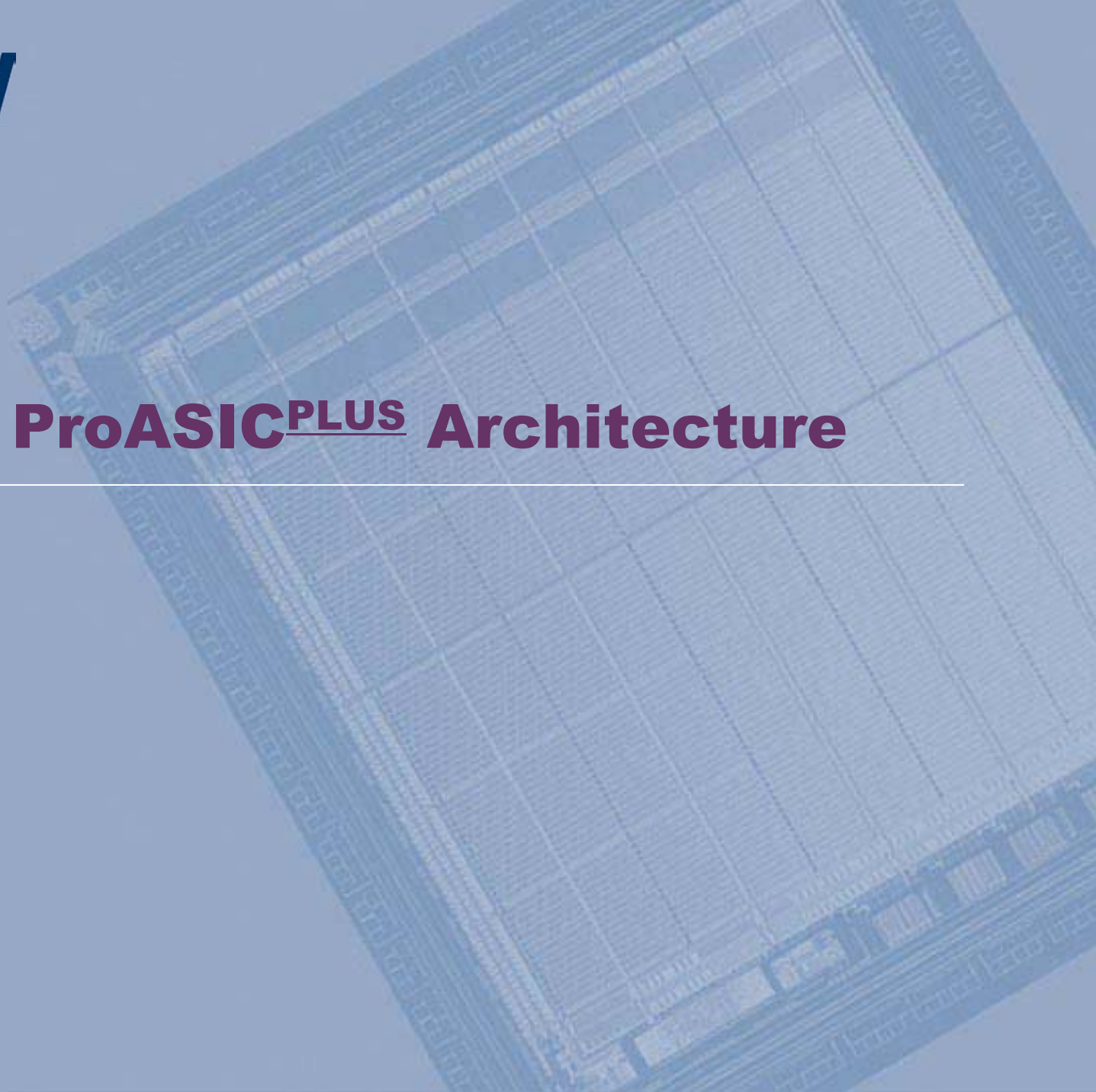




*Additional Hardware required



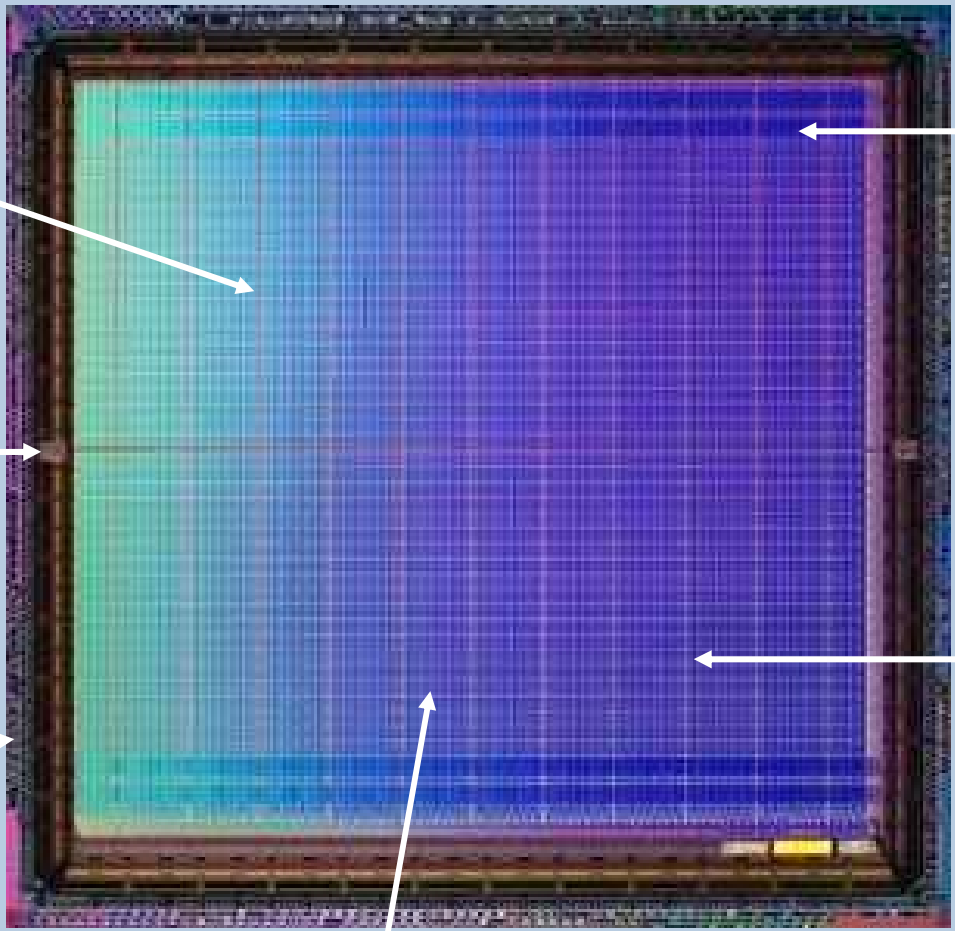
ProASIC^{PLUS} Architecture



ProASIC PLUS Chip Layout

The APA1000 has over 12 million Flash cells

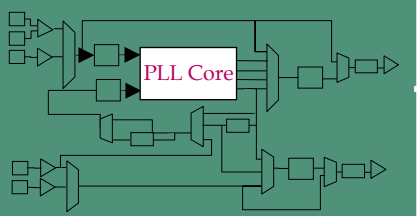
56,320 tiles of programmable logic



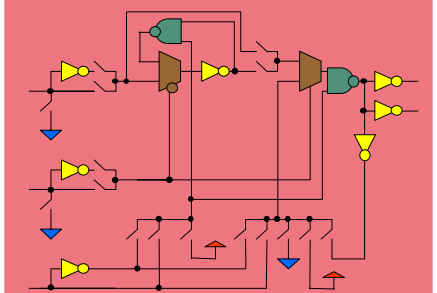
Basic RAM or FIFO Block 256 x 9

202,752 bits of configurable SRAM

PLL



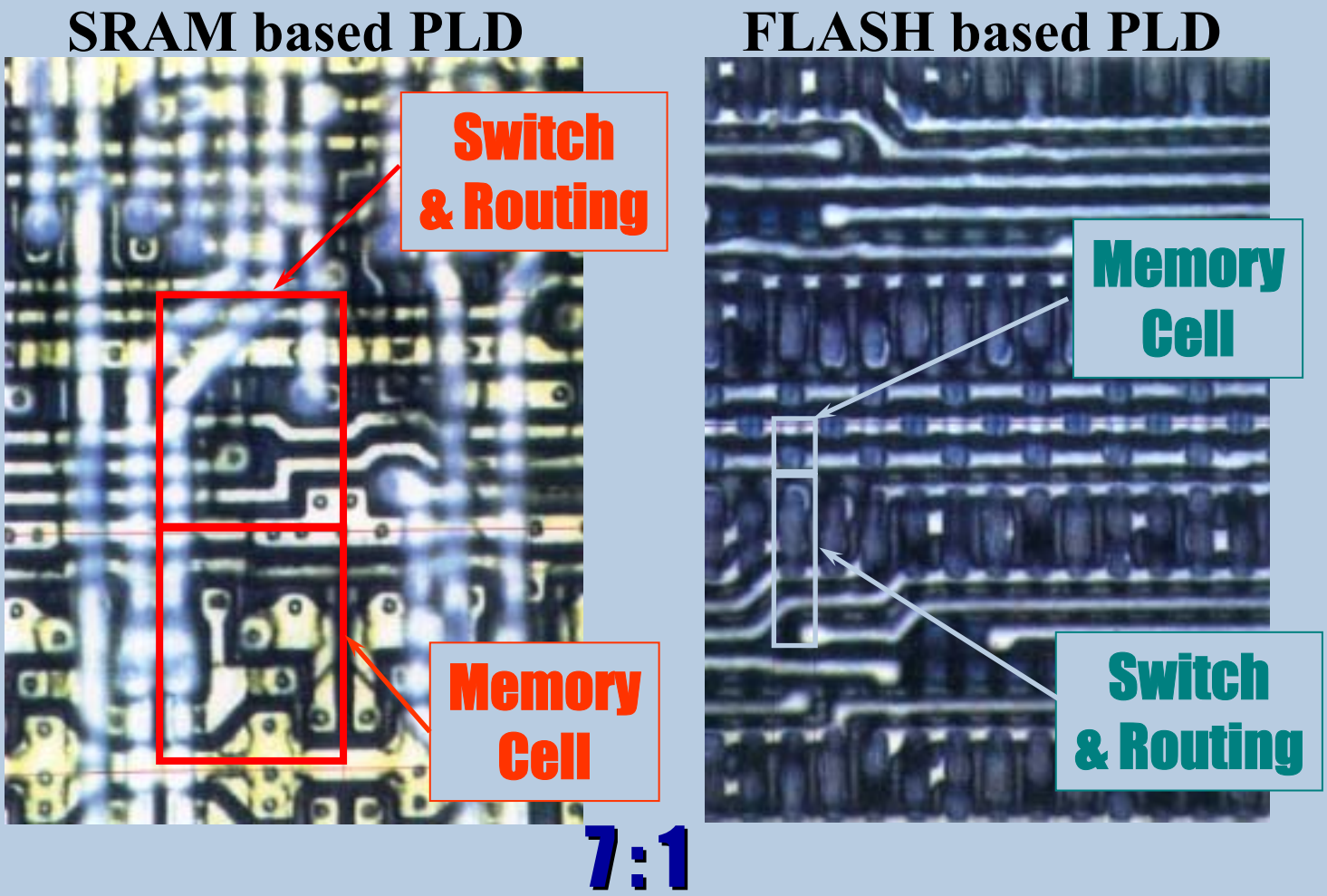
Logic Tile



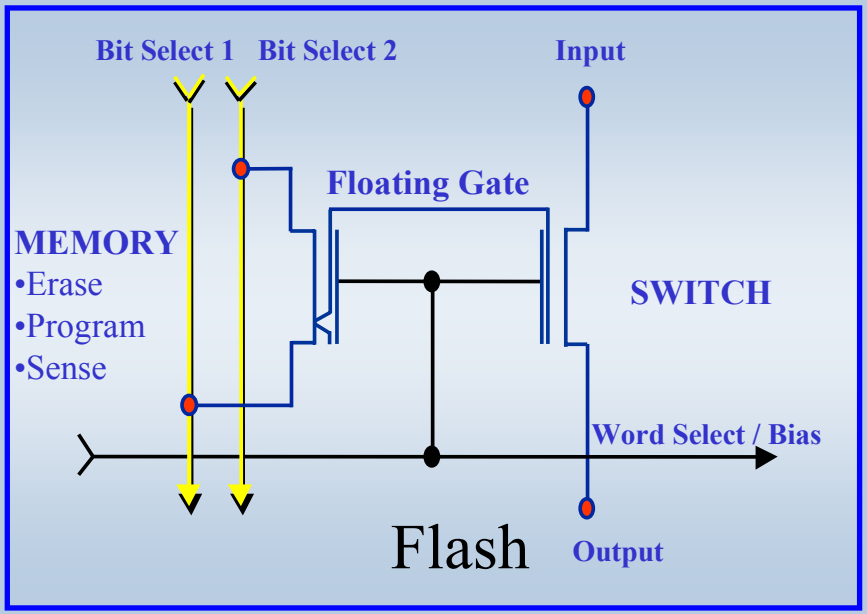
992 pads in the I/O ring

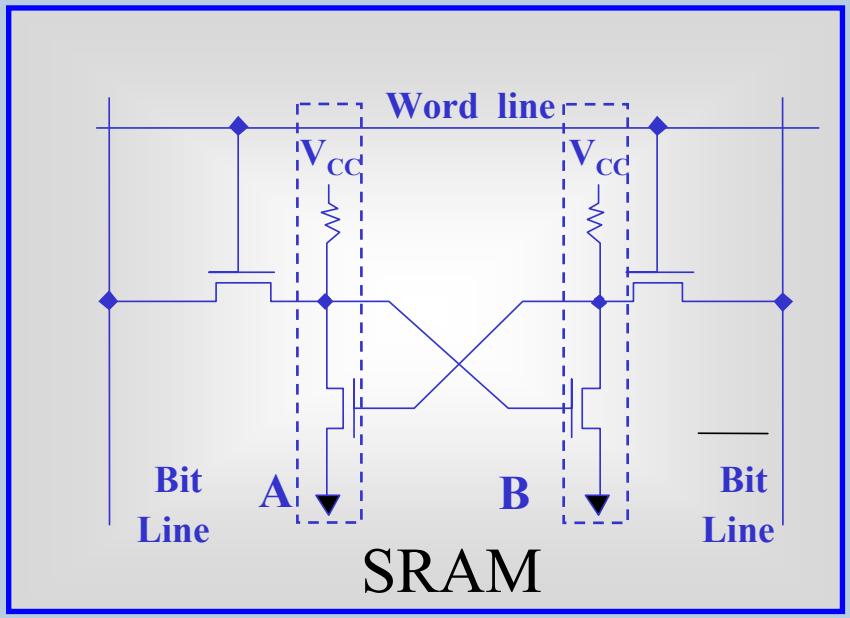
1,140,812 lines of interconnect for routing resources

SRAM Versus Flash
Switch & Memory Size



Flash Switch



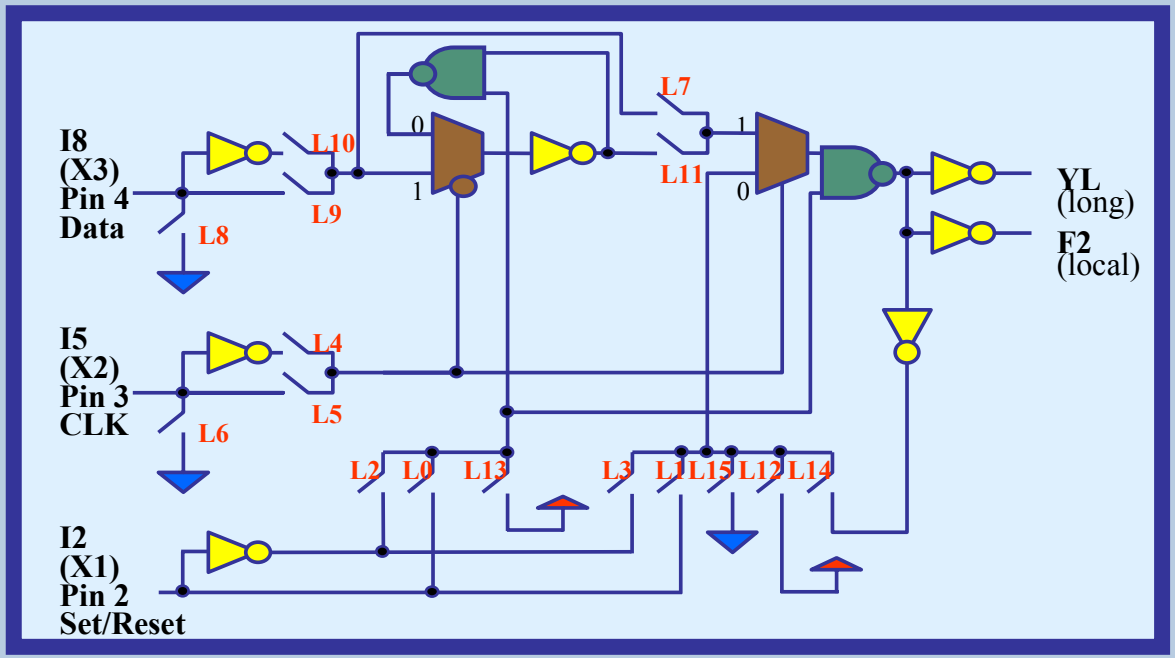


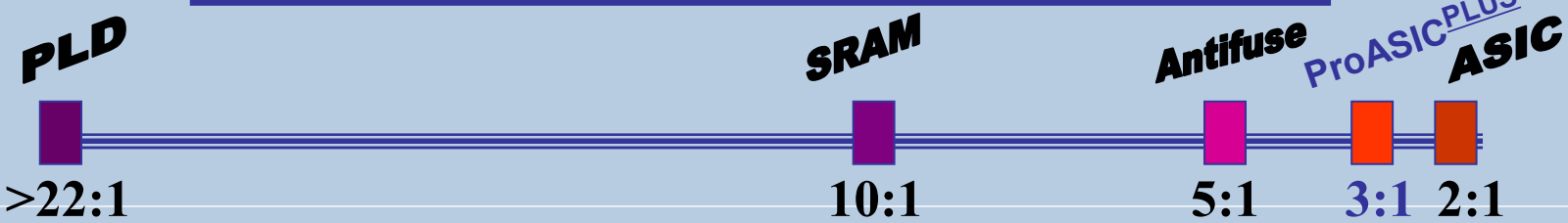
Flash Advantages

- Smaller size - more switches for greater routing flexibility
- Low power: less capacitance and resistance
- Re-programmable and non-volatile!

ProASIC^{PLUS} Fine Grained Architecture

Allows use of existing standard ASIC design flow and ASIC synthesis without architecture-specific mapping

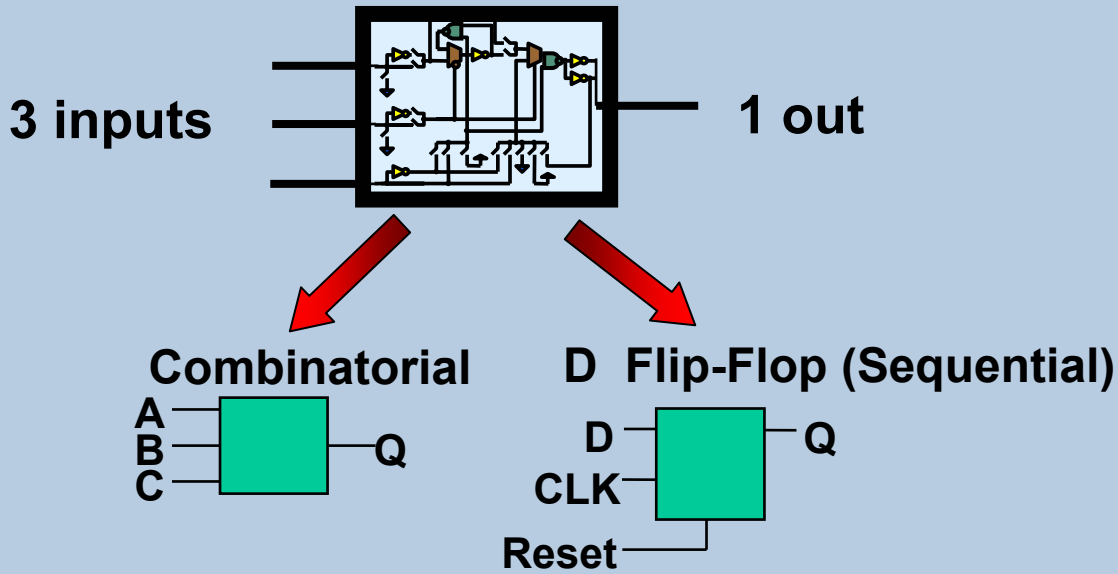




ProASIC^{PLUS} Core Tile

Every possible 3-input 1-output logic function can be implemented (except a 3-input XOR)

- The tile can map either a 3 input complex combinatorial gate, a latch or a D flip flop
  - Register intensive applications are handled easily
- All input signals can be inverted
  - Easier technology mapping and netlist optimizations



ProASIC^{PLUS} Routing Resources

High-performance routing hierarchy

- Low-skew global networks (four)
- Many high-speed very long lines
- Efficient long lines (1, 2 and 4 tiles long)
- Ultra-fast local routing (tile to tile)

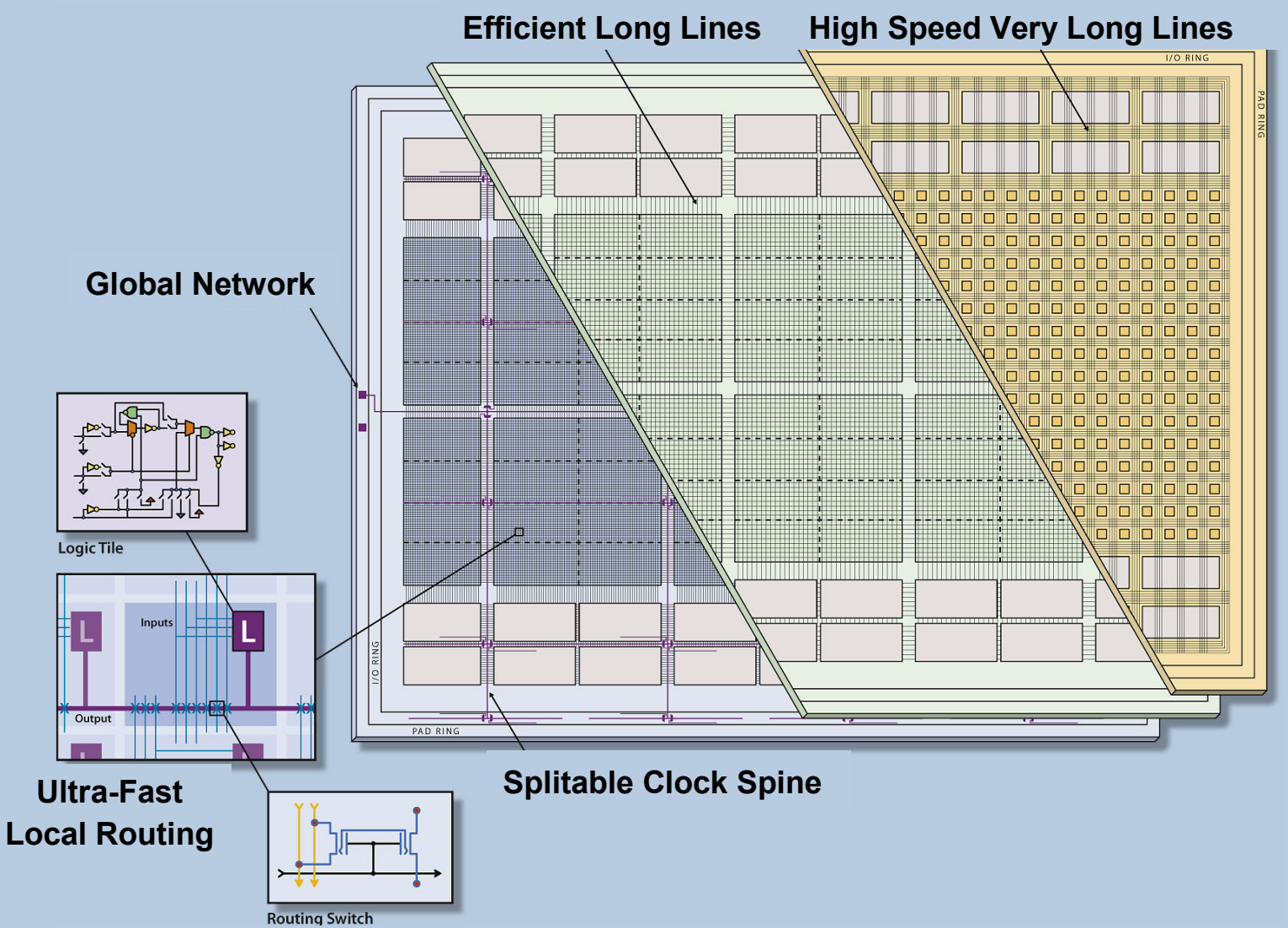
Small Flash switch advantage

- High switch count with compact physical layout
- Allows use of existing standard ASIC design flow and synthesis tools w/o architecture-specific mapping
- Enables ASIC-like timing and utilization predictability

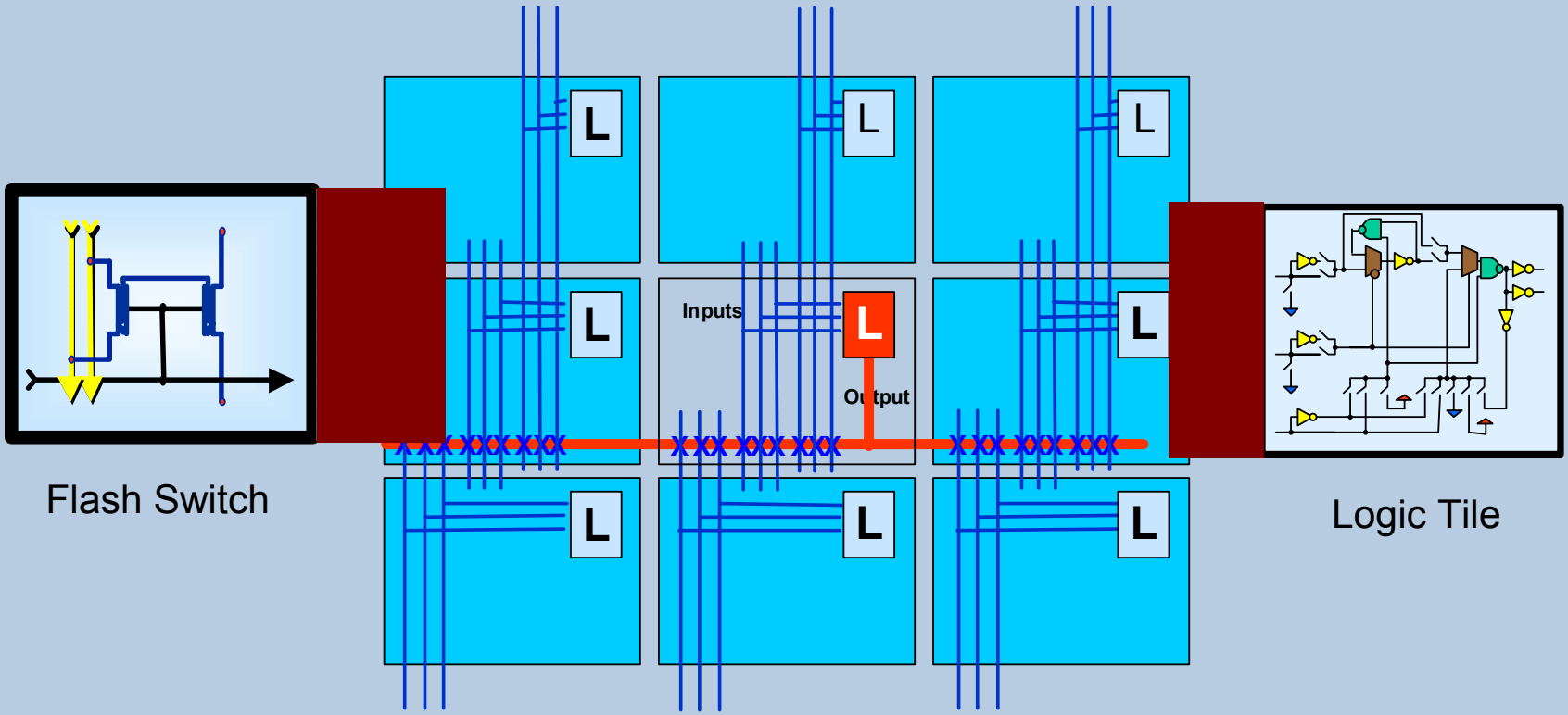
High efficiency and flexibility

- Multiple routing path alternatives for low congestion
- Short corner-to-corner delays

ProASIC PLUS Hierarchical Routing

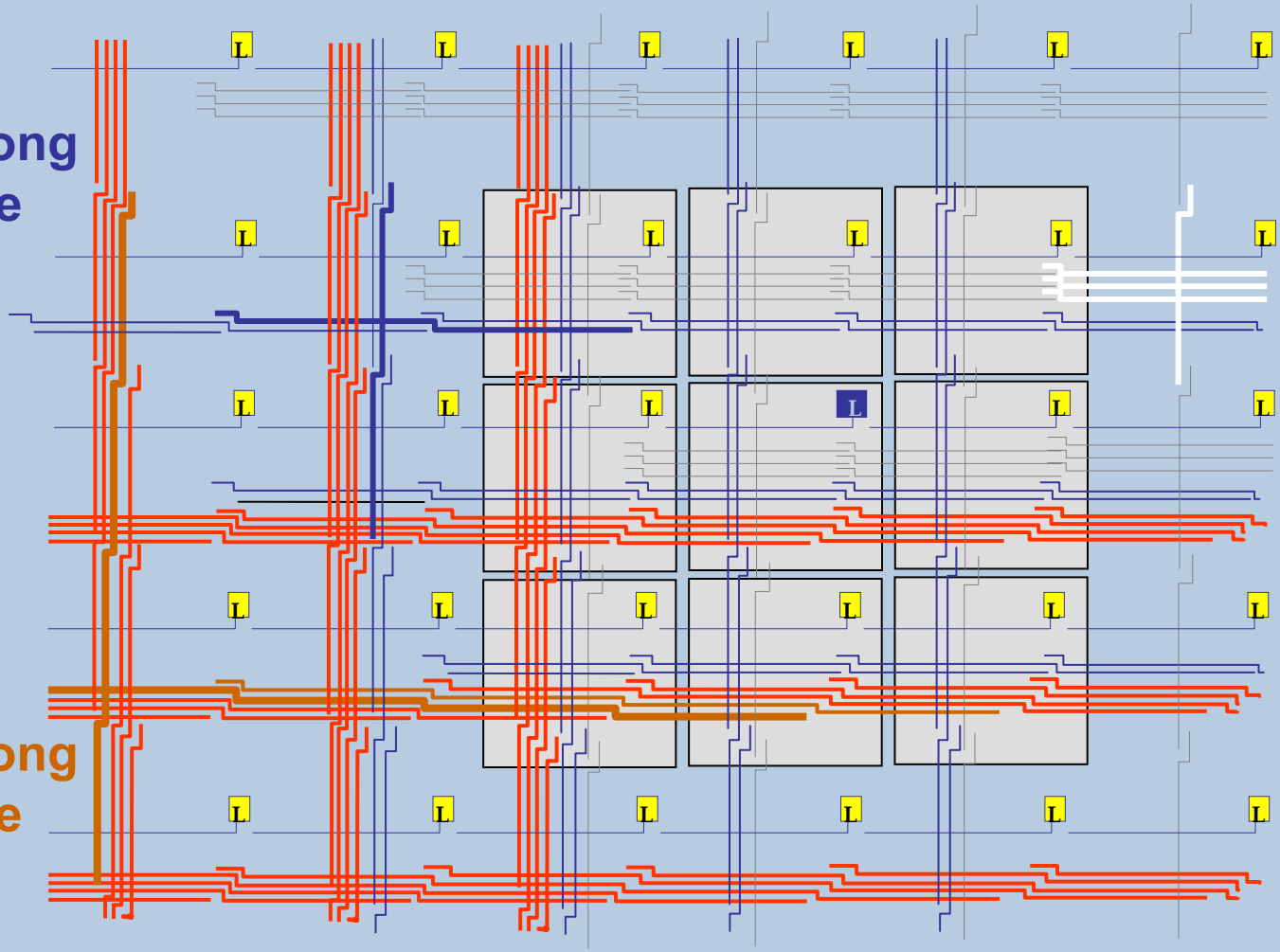


Ultra-Fast Local Routing

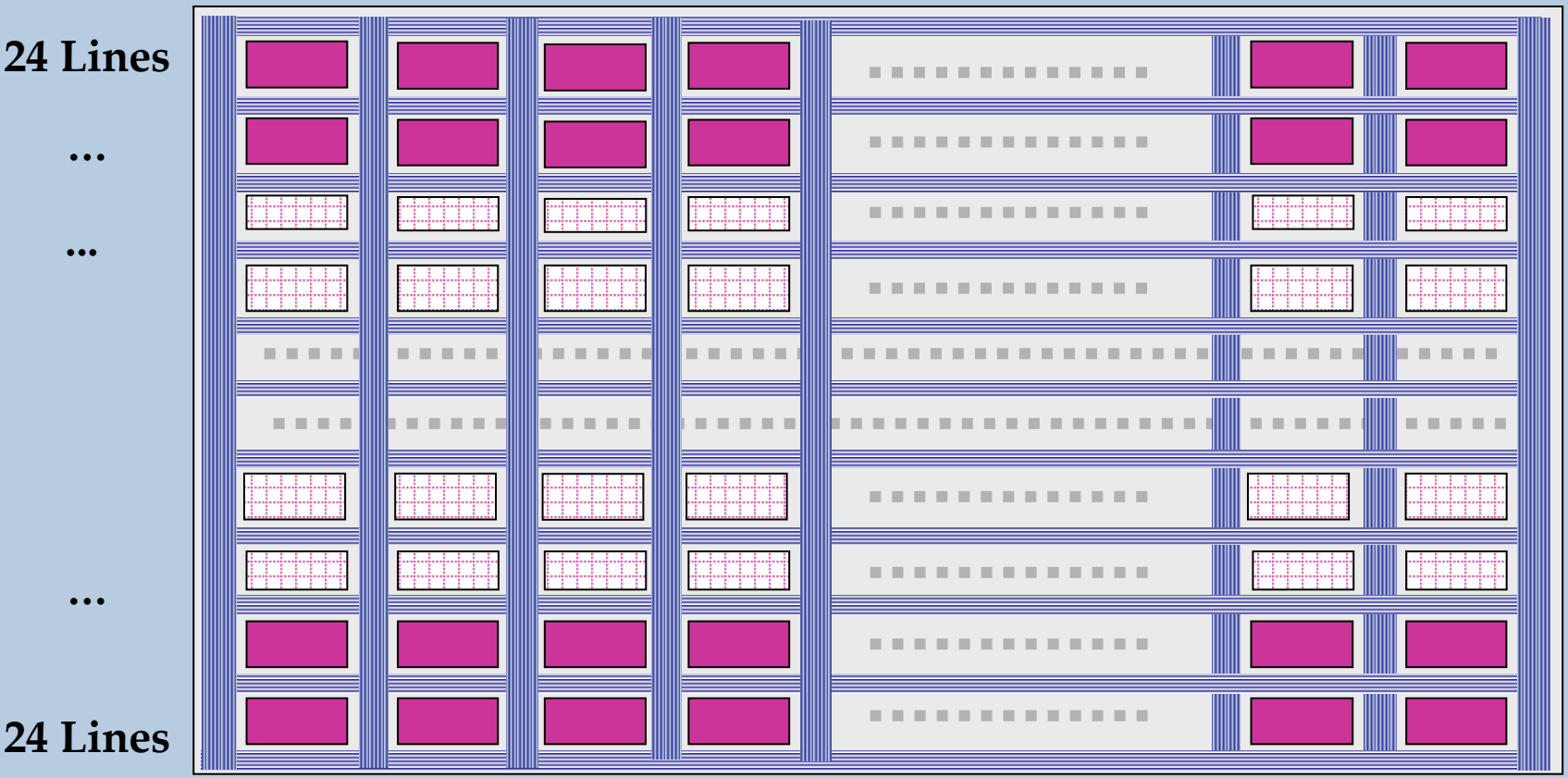


PLA-like, high-performance direct interconnect which allows the tile output to feed all 8 neighbors

Efficient Discrete Long Lines

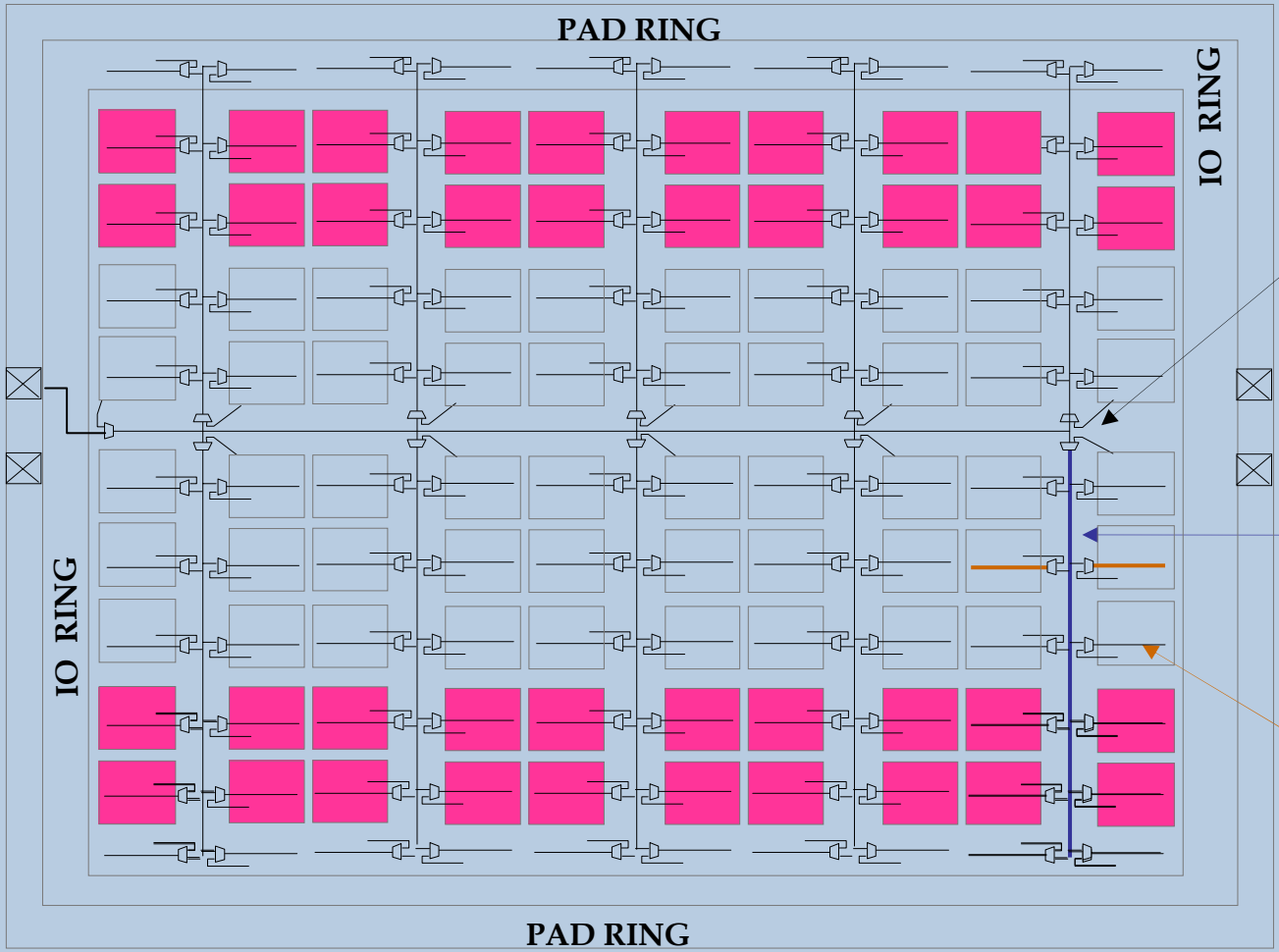


High-Speed Very Long Lines



Abundant interconnect options are provided by the large amount of Very Long Line routing paths across the entire chip

Low-Skew Global Routing



Bi-directional Global Pad

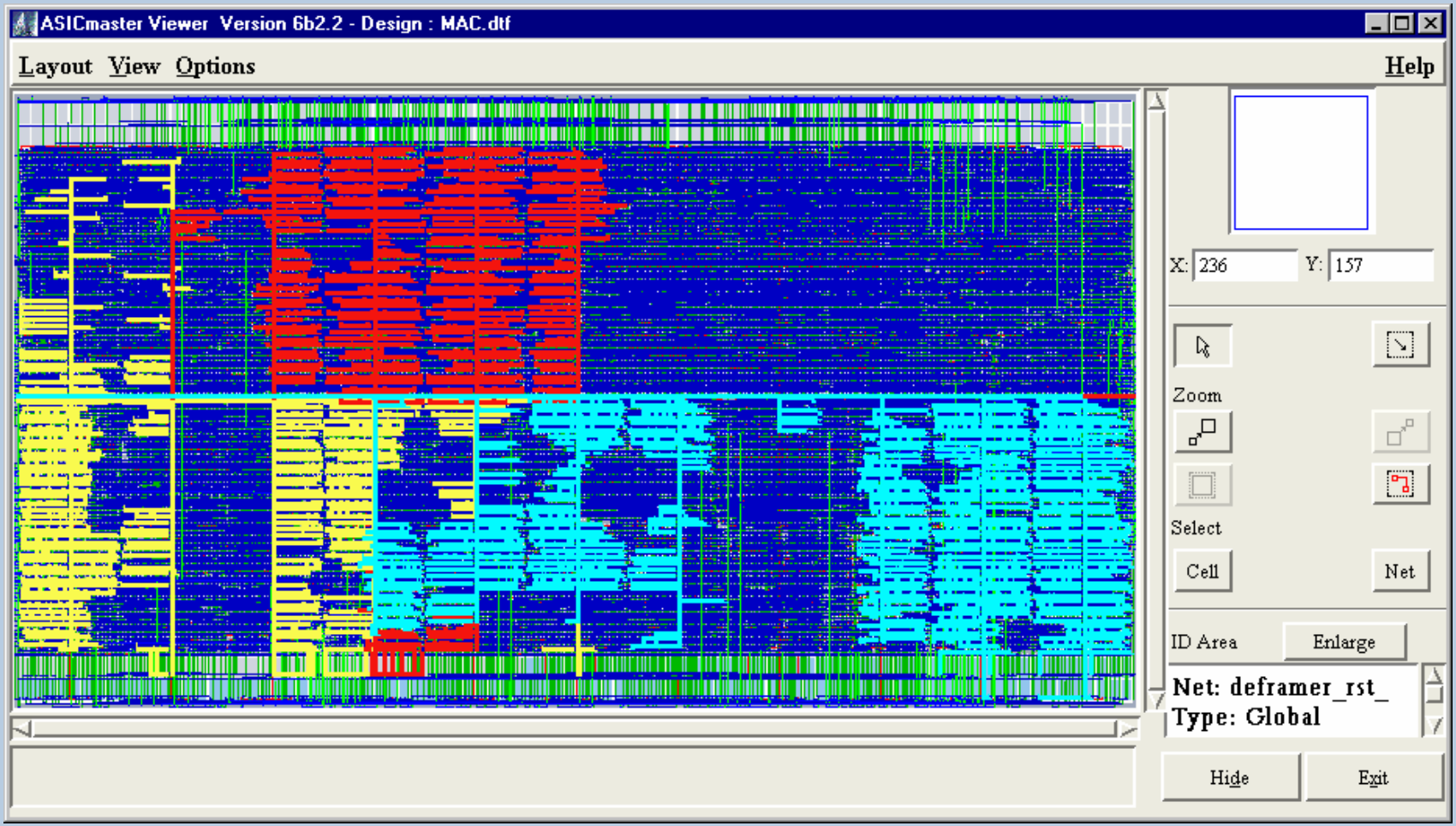
Low Skew Global Network

Global Spine

Global Ribs

Maximum skew less than 200 picoseconds

Clock Spines Split



Up to 88 separate segments for different clock systems are available

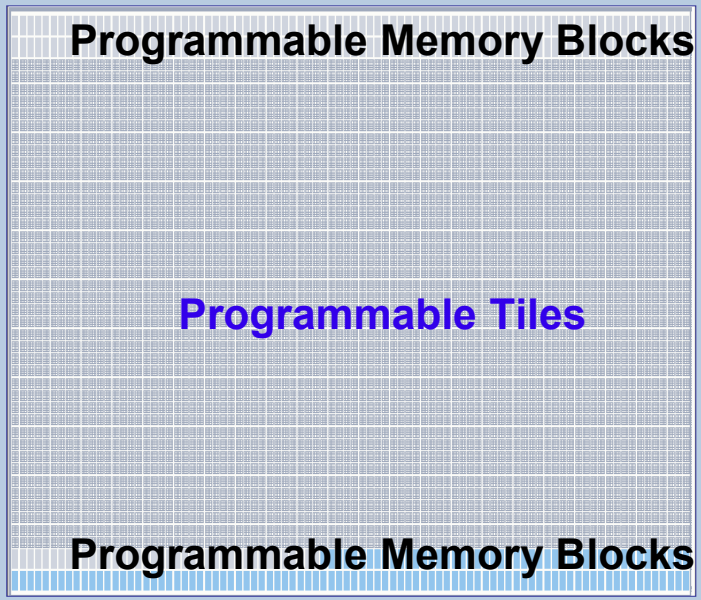
ProASIC^{PLUS} Embedded Memory

Two-port SRAM and FIFO capability

- Parameters and configuration fully programmable
- Synchronous or asynchronous
- Cascadable up to x wide by y deep
- ACTGen tool automates memory generation

16 to 88 embedded memory blocks (256x9) with:

- 1 read and 1 write port
- Decoder logic
- Control and flag circuitry
- Parity generation
- Detection logic
- Access and cycle time <7ns



Embedded Memory Blocks

Two-port SRAM and FIFO capability

ACTgen tool automates memory generation

- Parameters and configuration fully programmable

1R/1W 256x9 embedded memory block

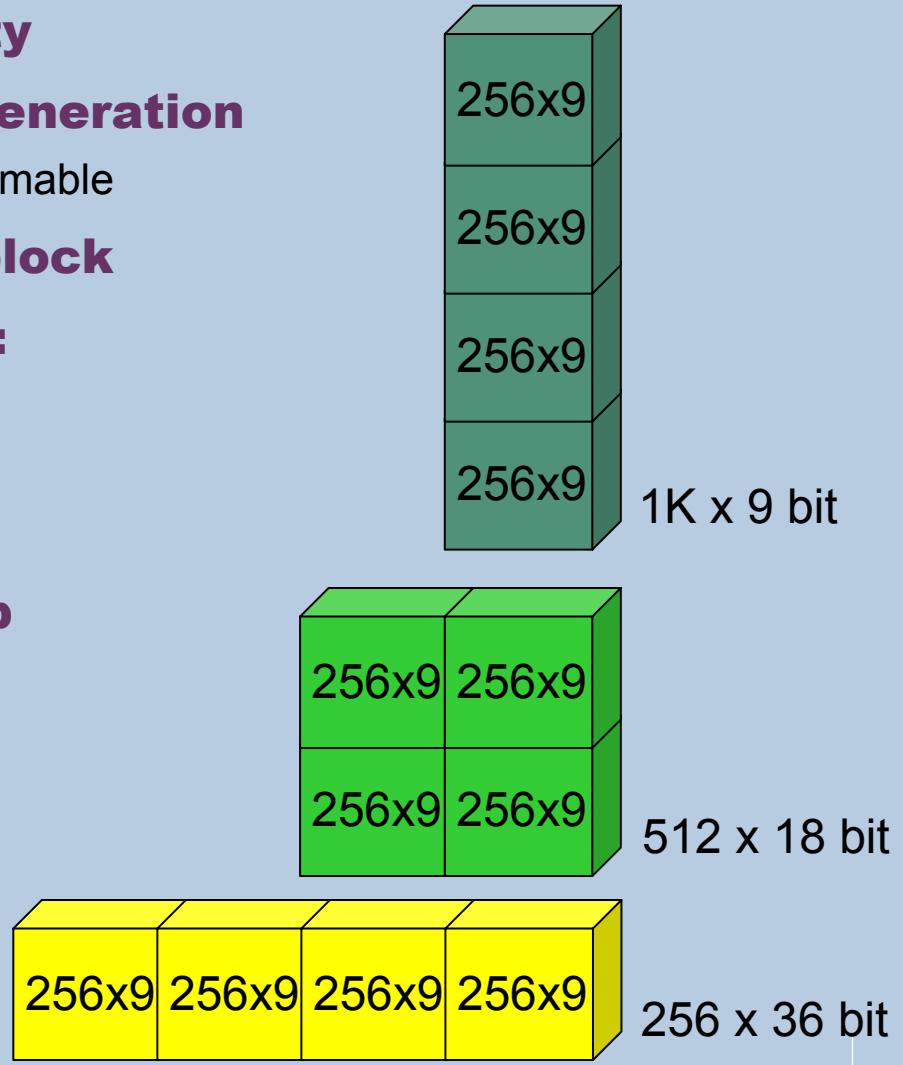
With embedded FIFO control logic:

- Decoder, control and flag circuitry
- Parity generation/detection logic
- Static and dynamic triggers

Cascadable up to x wide by y deep

Programmable as synchronous or asynchronous

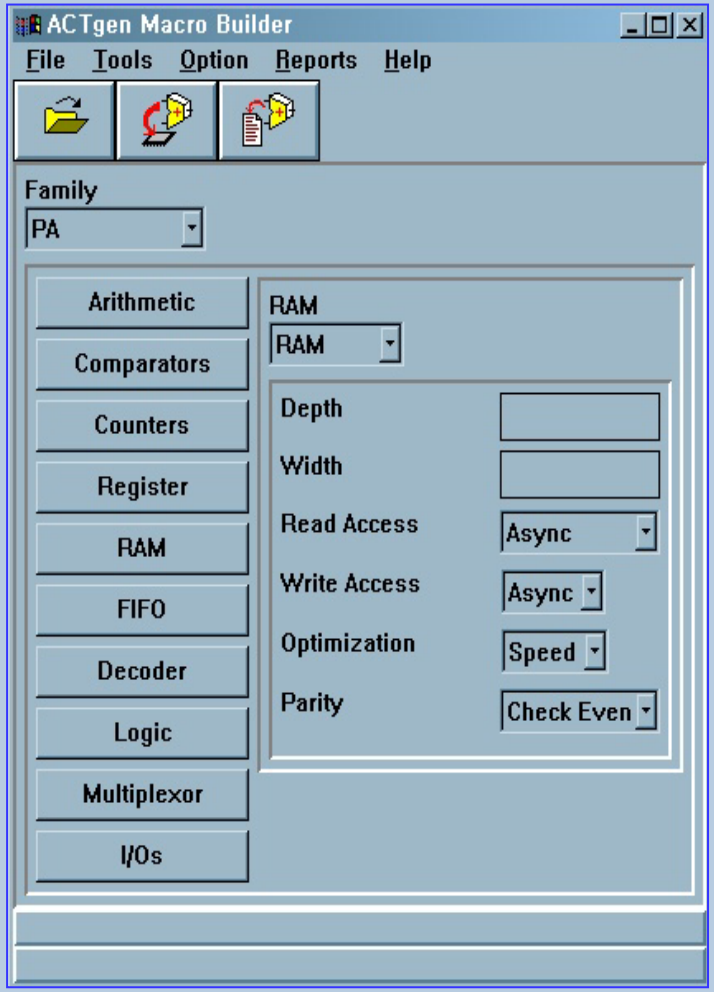
Can not split



ACTgen Features

Includes

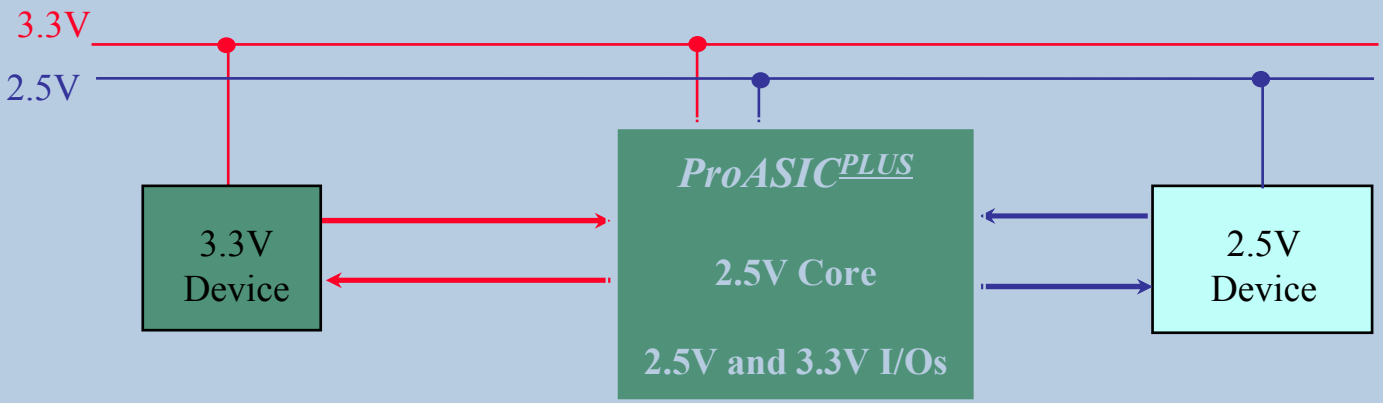
- Embedded Memories Builder(EMB) : creates memory blocks using Embedded memory blocks
- Distributed Memories Builder(DMB) : creates memory blocks using Logic Tiles
- User can select different options
  - FIFO or RAM
  - synchronous or asynchronous
  - width and depth
  - parity/no-parity
  - polarity of Read and Write clocks
- User can instantiate these memories into the design
- Supported netlist formats
  - EDIF, VHDL and VerilogHDL



ProASIC^{PLUS} I/Os

Design driven performance features

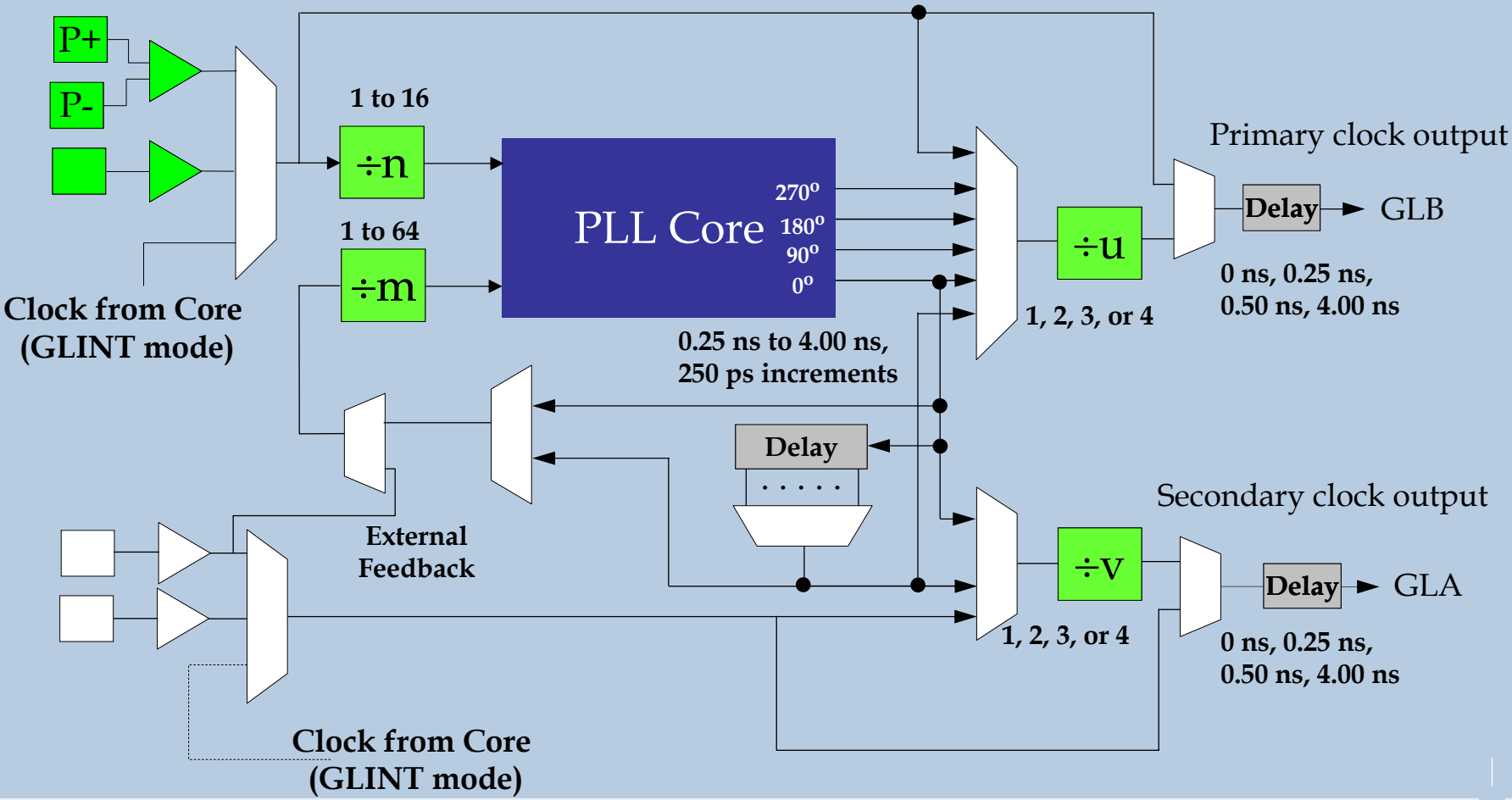
- Separate I/O and core power rings
- Individually selectable 3.3V & 2.5V I/Os
- 3.3V PCI up to 50 MHz
- Two LVPECL differential pairs (Clock & Data)
- Bi-directional Global Pads (Clocks, Resets, Critical PCI Signals)
- Programmable Schmitt Trigger on Inputs
- Slew-rate control: 25 mA/nsec, 50 mA/nsec, 100 mA/nsec



Clock Conditioning Circuitry Block Diagram

Primary Clock Delay -4ns to +8ns

Secondary Clock Delay -4ns to +8ns



PLL Characteristics

Input frequency range	1.5 - 240 MHz
Feedback frequency range	1.5 - 240 MHz
Output frequency range	6 to 240 MHz
Maximum output clock jitter	200 ps at 50 ps jitter of f_{in}
Maximum acquisition time	20 us
Delay Line	Programmable in 250 ps increments from -4 ns to 8 ns
Output Phase Shift	0^o, 90^o, 180^o, 270^o
Output Duty Cycle	50%

ProASIC^{PLUS} ISP

In System Programming

- Microprocessor interface option for ProASIC^{PLUS} programming
- On circuit board DC to DC converters can be implemented to supply the programming voltages
- ProASIC^{PLUS} core power remains connected during programming
- Portable or production programmers using a direct JTAG interface can also be used for ProASIC^{PLUS} programming, on or off the board

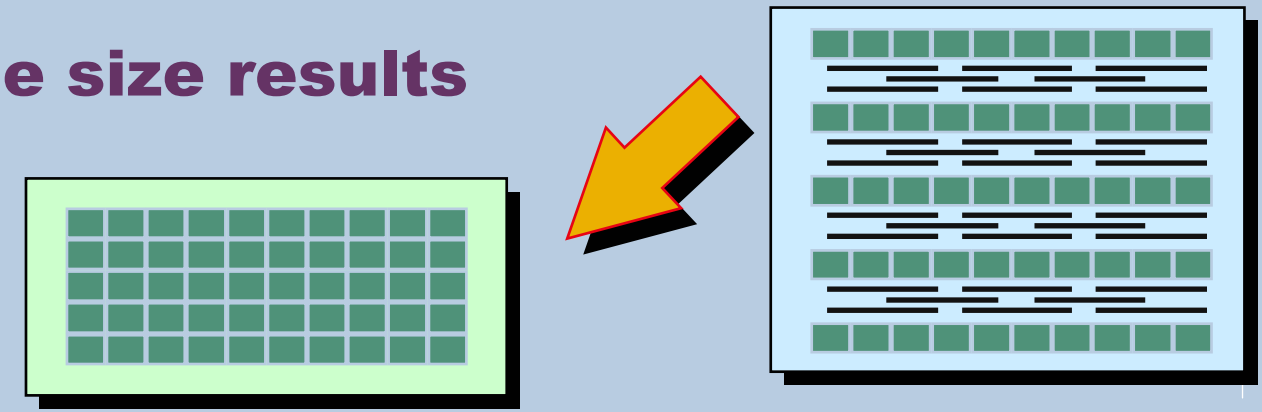
Design Security

- ProASIC^{PLUS} does not require an external bit stream from a processor or boot PROM — no bit stream to be copied
- Devices are user programmed with a multi-bit security key that prevents non-key holders from reading or altering the configuration settings (up to 263 bits)
- Decapping and stripping a device only reveals the structure of the device, not the contents of the flash cell
- Competing technologies offer much lower levels of protection for valuable IP

Antifuse Architecture

SXA/SX/eX Architecture

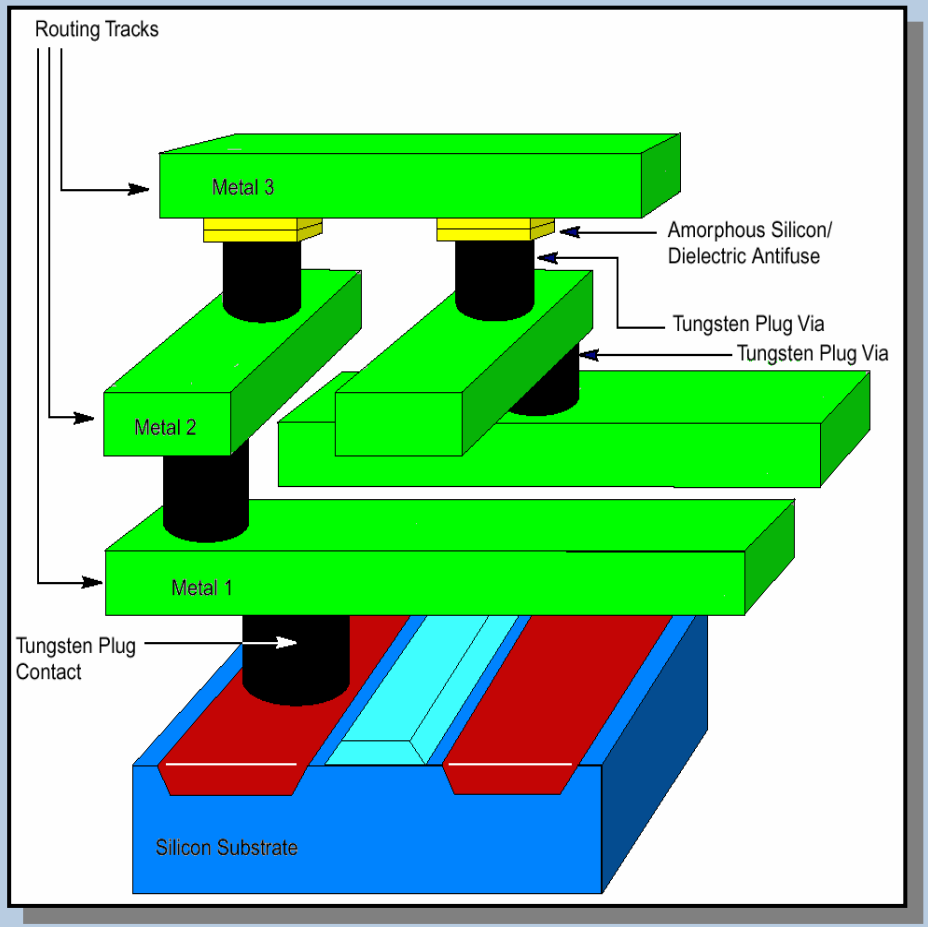
- Sea-of-modules architecture
- Routing interconnect rests above logic resources
- Minimum silicon area is devoted to routing resources
- Logic resources are tightly packed onto silicon
- A very small die size results



eX Technology

Sea-of-modules architecture based on metal-to-metal antifuse

- Switching element (antifuses) reside between the last two layers of metal, above the logic resources
- Fast signal propagation
  - Antifuse connection has less than 1fF capacitance and 25 Ohms resistance

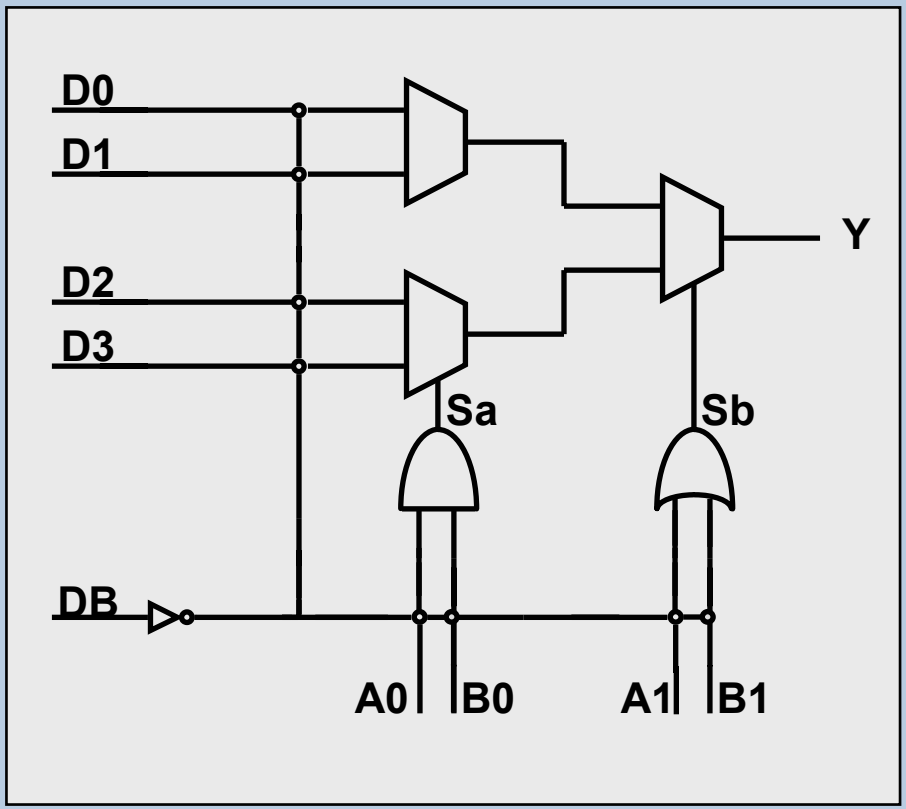


eX Architecture

Synthesis-Friendly C-Cell, R-Cell Structures

- Combinatorial Cell (C-Cell)
  - Flexible cell design
  - Combinatorial functions up to 5 inputs
- Register Cell (R-Cell)
  - Flip-flops separate from combinatorial logic
  - Direct connect with C-Cell for fast setup time
  - Asynchronous clear and preset

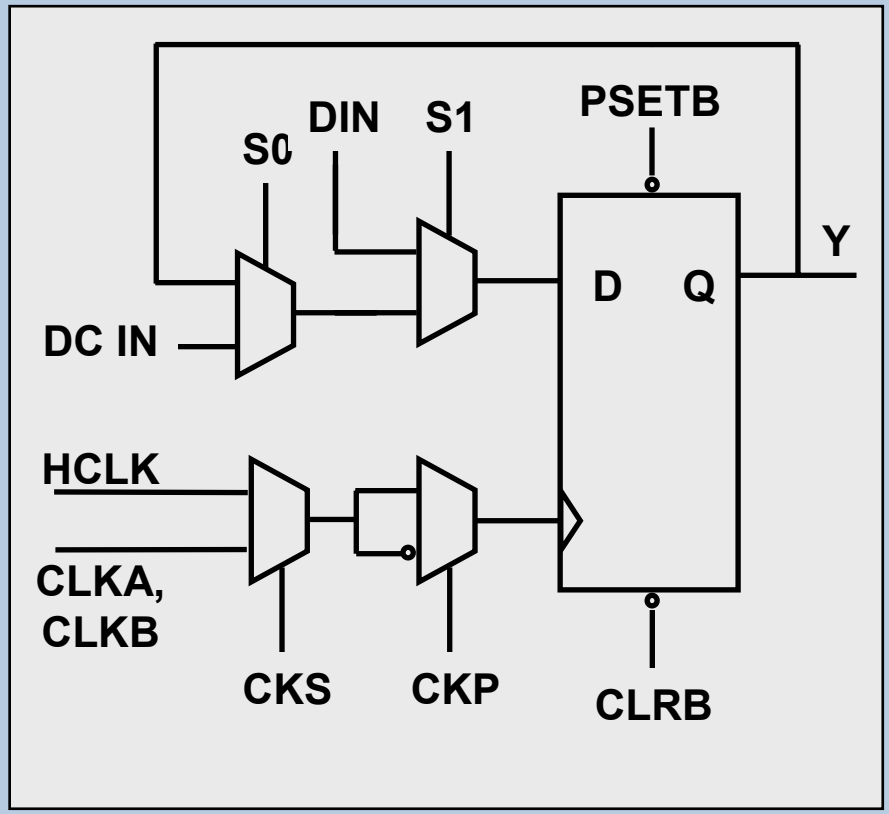
eX Architecture: C-Cell



- 2 level MUX structure
- 4 data inputs (D0-D3)
- 4 controls (A0, A1, B0, B1) accessible by routed clocks (CLKA, CLKB)
- Ability to invert any input (using DB)
- Over 4,000 possible functions up to 5 bits

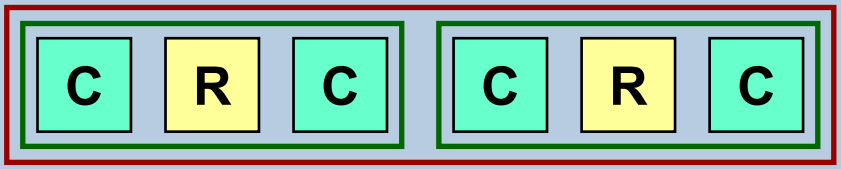
eX Architecture: R-Cell

- Direct-Connect to adjacent C-Cell for fast setup time (DC IN) or independent connection to other logic cells and I/Os (DIN)
- Asynchronous reset (PSETB) and clear (CLRB)
- Connect to hardwired fast clock (HCLK) or routed clock (CLKA, CLKB)
- Choice of clock polarity
- Embedded clock enable

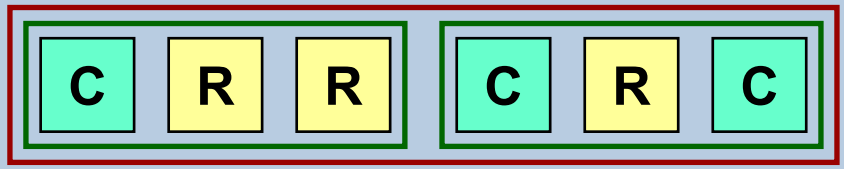


Super Clusters

Type 1 *Super Cluster*



Type 2 *Super Cluster*



- Each Cluster Consists of C-R-C or C-R-R
- Each Super Cluster Consists of 2 Clusters
- Extremely Fast, Flexible Interconnect
  - Direct Connect between C-Cell and R-Cell
  - Fast Connect within each Super Cluster
  - Fast Connect between each Super Cluster and the Super Cluster immediately below

New I/O Features

- Mixed-voltage support (2.5V, 3.3V, 5.0V)
- 3.3V & 5V PCI support
- 2.5V, 3.3V and 5.0V I/O drive capability
- Hot-swapping support
  - Power-up/down-friendly I/Os (no sequencing needed)
- Tri-stated I/Os during power-up
- Individual slew control on I/Os
- Four additional clock domains in SX72A
- Optional JTAG RESET pin on all devices

Hot-Swapping

What is it?

- Live insertion/removal, hot plug, hot insertion, hot swapping

Where is it used?

- Networking, fault-tolerant computing, telecom infrastructures

What factors define hot-swapping functionality?

- Able to draw no current while power supply is off, but I/Os receive power
- Power-up sequence friendly
- Output driven to HZ until valid data is defined at pre-driver
- No DC load to host bus
- No damages or reliability issues result from using the device