design & verification conference & exhibition

February 24 - 26, 2003

Speed Up Verilog Simulation By 10-100x Without Spending A Penny

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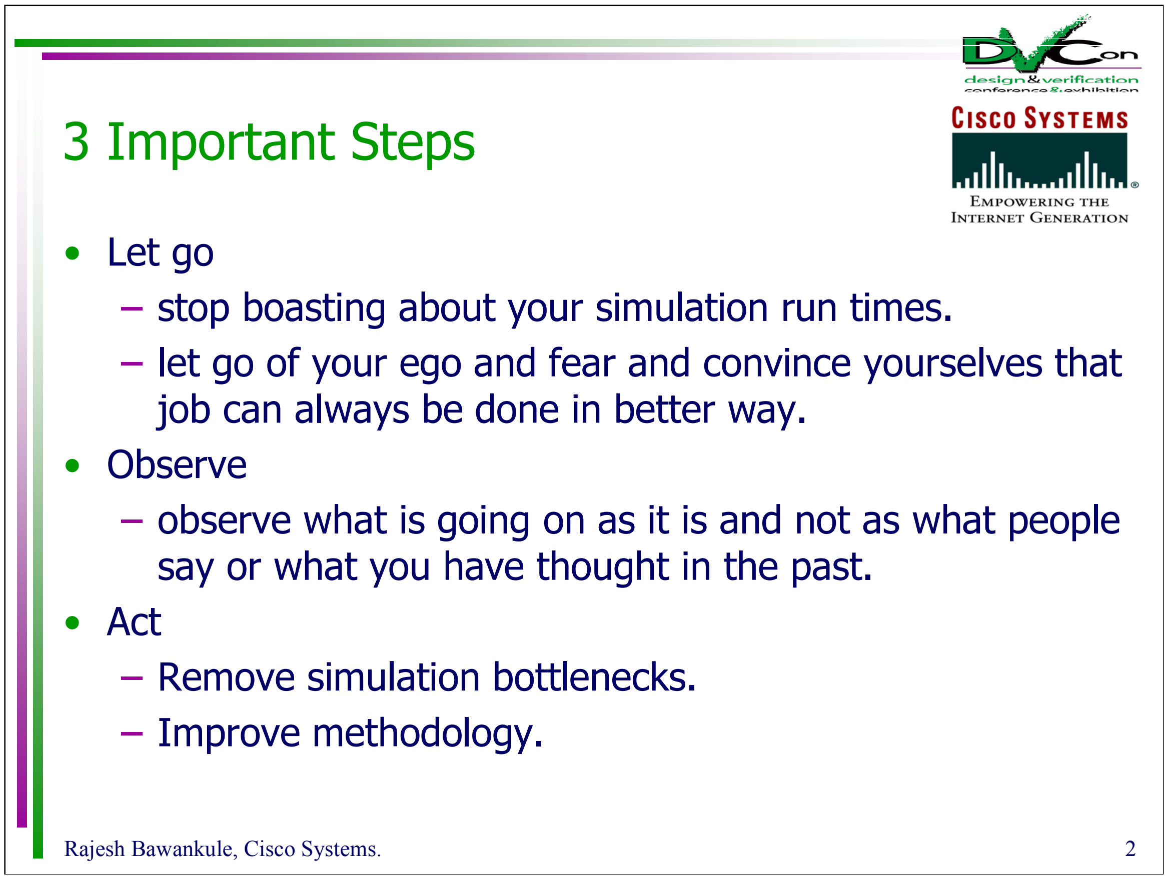
1



3 Important Steps

- Let go
  - stop boasting about your simulation run times.
  - let go of your ego and fear and convince yourselves that job can always be done in better way.
- Observe
  - observe what is going on as it is and not as what people say or what you have thought in the past.
- Act
  - Remove simulation bottlenecks.
  - Improve methodology.

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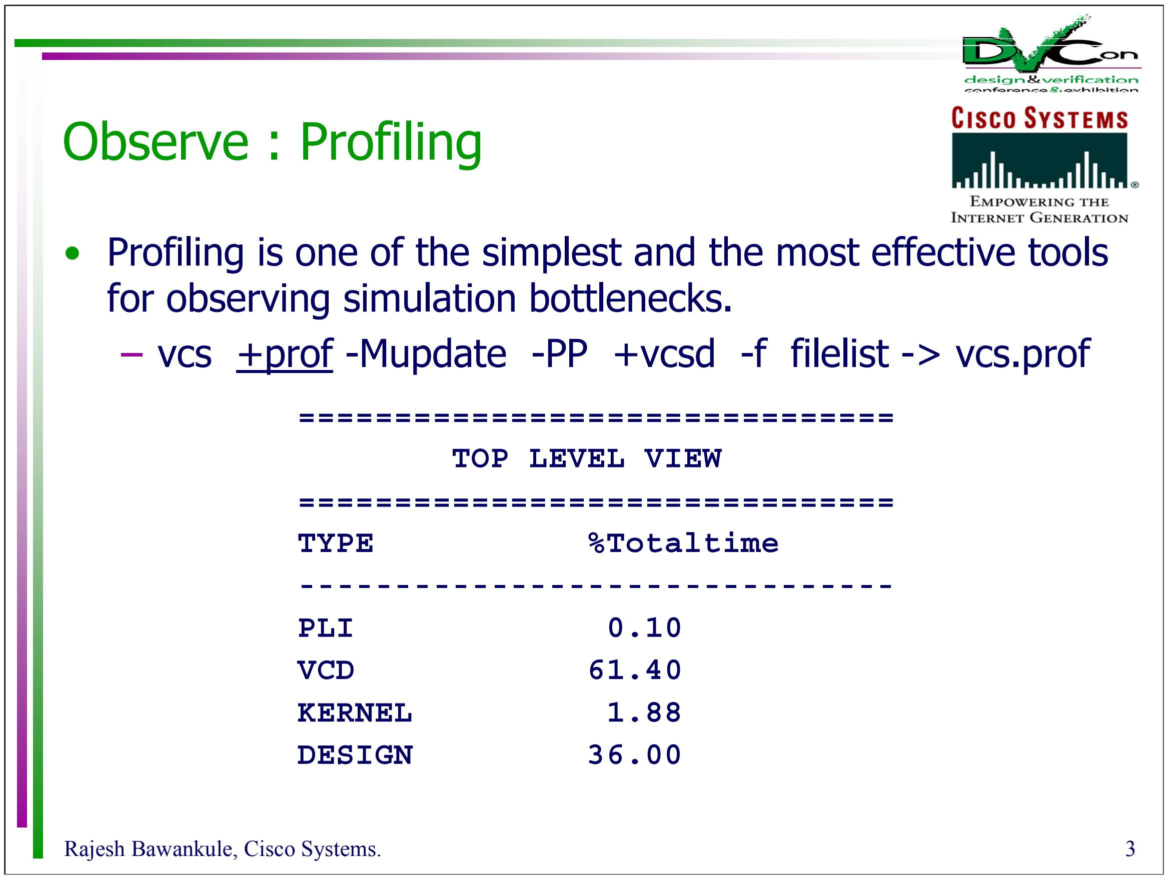

Observe : Profiling

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- Profiling is one of the simplest and the most effective tools for observing simulation bottlenecks.
  - vcs +prof -Mupdate -PP +vcsd -f filelist -> vcs.prof

```
===============================
        TOP LEVEL VIEW
===============================
TYPE           %Totaltime
-------------------------------
PLI              0.10
VCD             61.40
KERNEL           1.88
DESIGN          36.00
```

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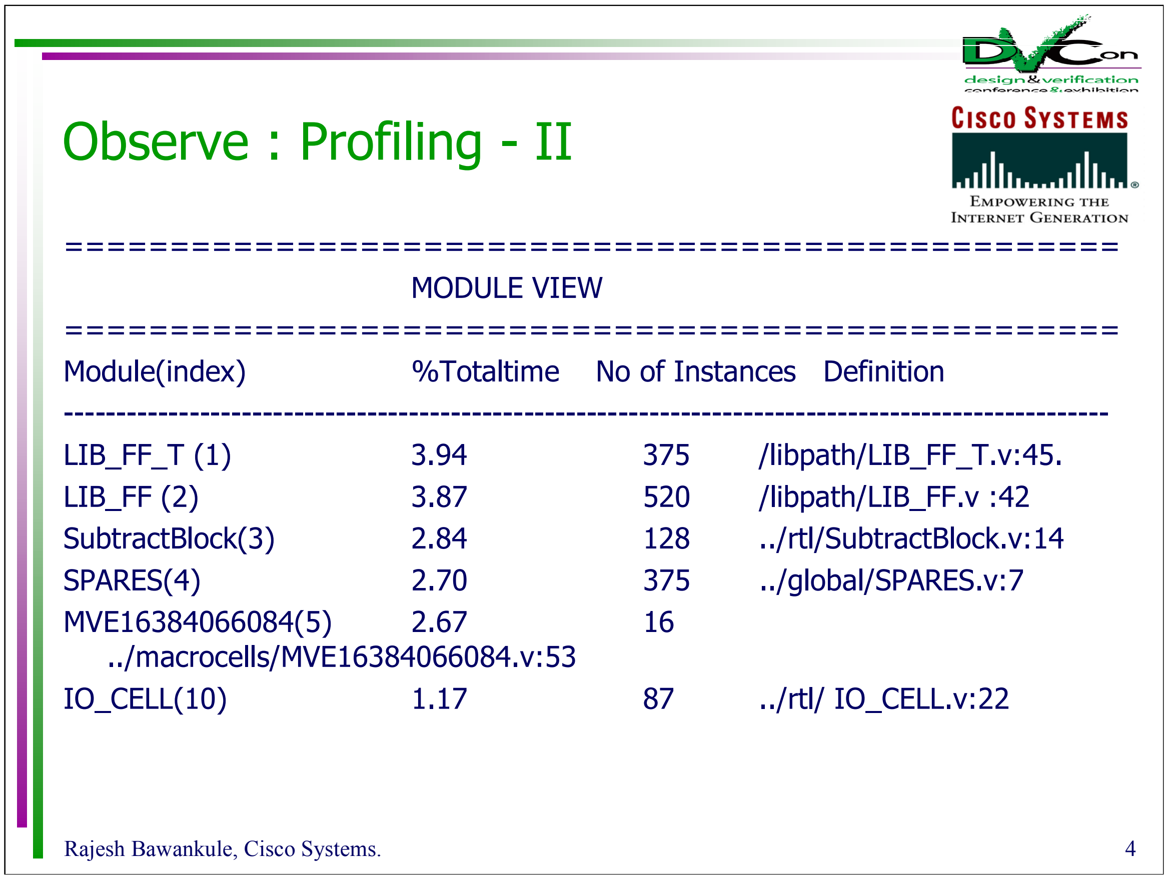
- This means that 60% time is spent in dumping the VCD file. Someone forgot to turn off the dumping switch! If we are running regressions then we need not keep this dumping on. Just turning off the dumping gave us 2x speed up.



Observe : Profiling - II

```
====================================================
                    MODULE VIEW
====================================================
Module(index)          %Totaltime   No of Instances   Definition
-----------------------------------------------------------------------------------------------
LIB_FF_T (1)           3.94         375        /libpath/LIB_FF_T.v:45.
LIB_FF (2)             3.87         520        /libpath/LIB_FF.v :42
SubtractBlock(3)       2.84         128        ../rtl/SubtractBlock.v:14
SPARES(4)              2.70         375        ../global/SPARES.v:7
MVE16384066084(5)      2.67         16
   ../macrocells/MVE16384066084.v:53
IO_CELL(10)            1.17         87         ../rtl/ IO_CELL.v:22
```

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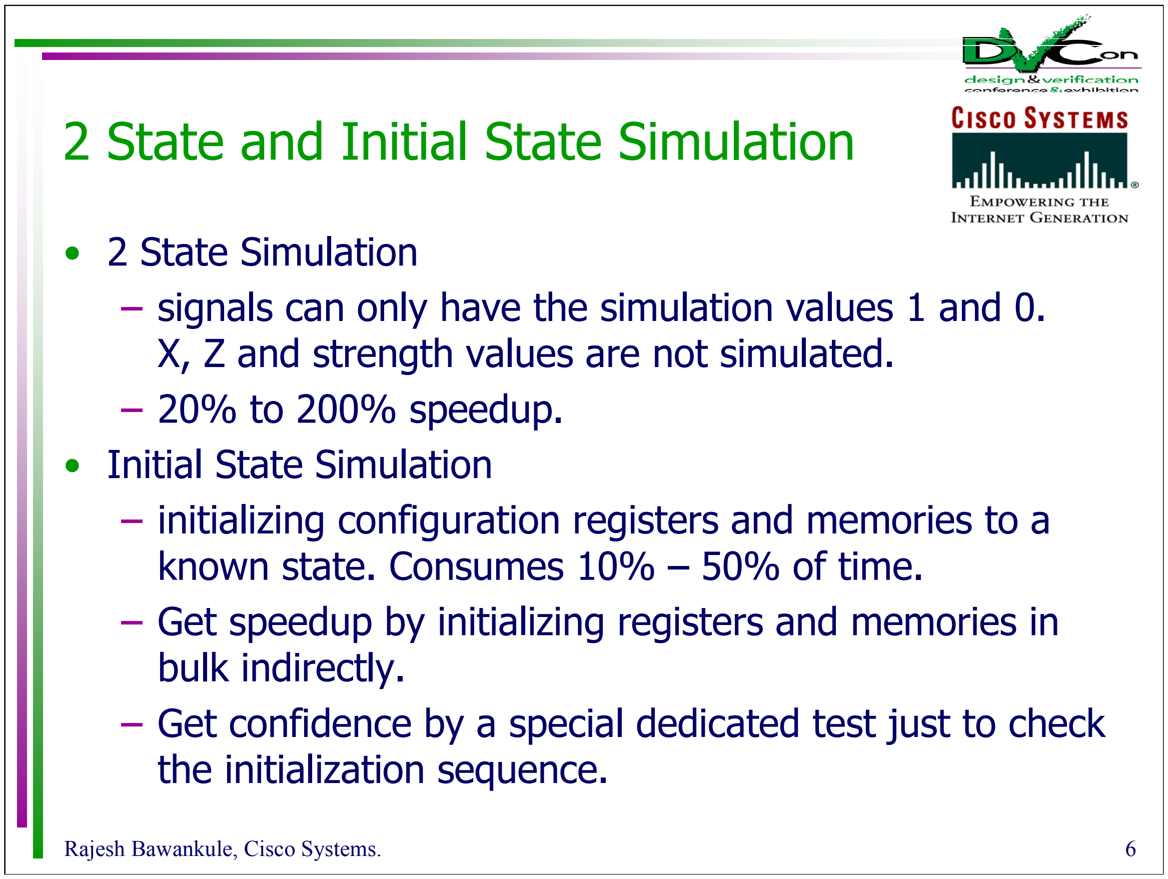
- 13-14% time is spent in 2 flops and the spare gates block. This means around 35% logic simulation time is spent on these gates. ((100/40) * 14). Well, at least for this test. Other tests will hammer some other portion of logic.

- Spare Gates as well as IO macro cells contained instances of flops and gates that do not get optimized after synthesis. I created a blank module for the spare gates and wrote a simpler model for the flipflop to reduce run times. Combined with not dumping I could get around 4x speedup.

Optimized compilations

- Synopsys VCS has inbuilt Radiant technology which can dramatically boost the simulation runs while running long regressions.
  - +rad or +rad+2 Specifies Radiant level 2
  - +rad+1 Specifies Radiant level 1
  - +optconfigfile applying optimizations to part of the design using a configuration file.
- Do not work with coverage tools or SDF back annotated simulations.
- 4x to 10x performance boost



2 State and Initial State Simulation

- 2 State Simulation
  - signals can only have the simulation values 1 and 0. X, Z and strength values are not simulated.
  - 20% to 200% speedup.
- Initial State Simulation
  - initializing configuration registers and memories to a known state. Consumes 10% – 50% of time.
  - Get speedup by initializing registers and memories in bulk indirectly.
  - Get confidence by a special dedicated test just to check the initialization sequence.

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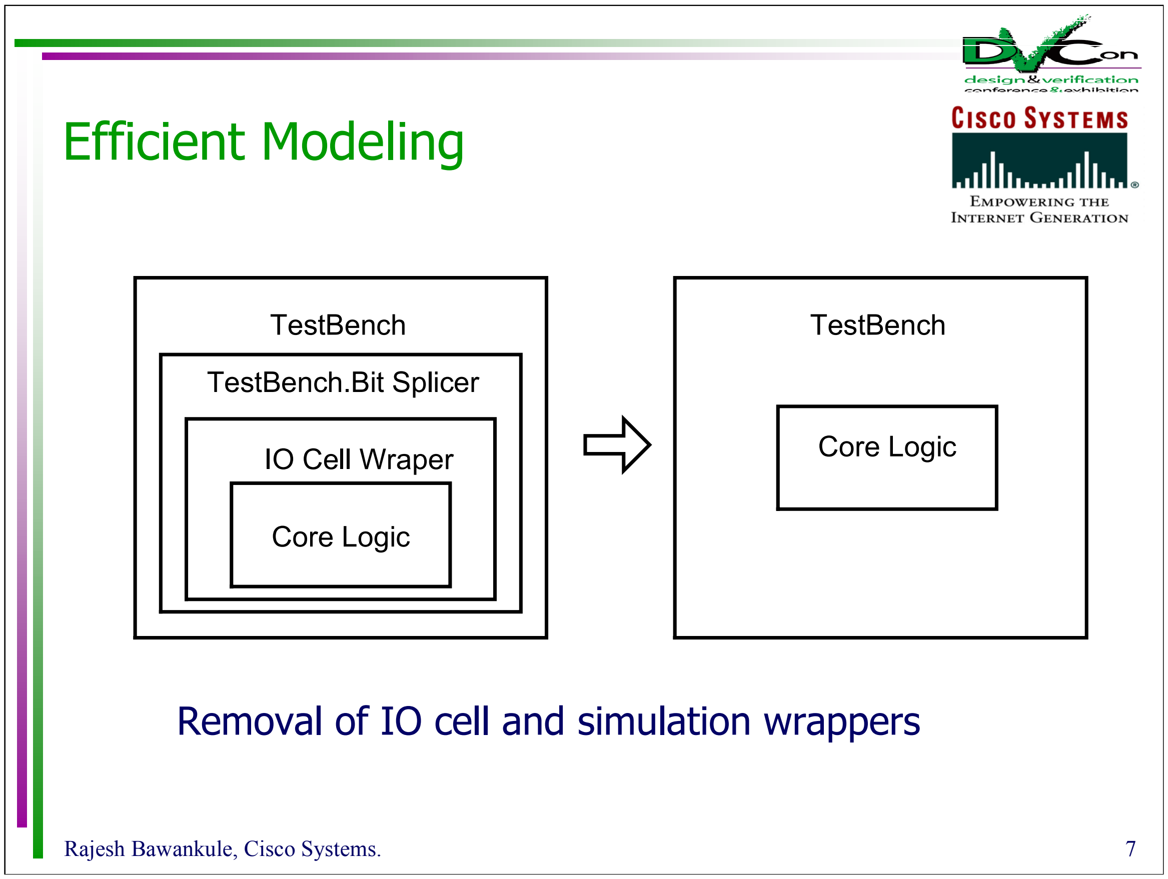

Efficient Modeling

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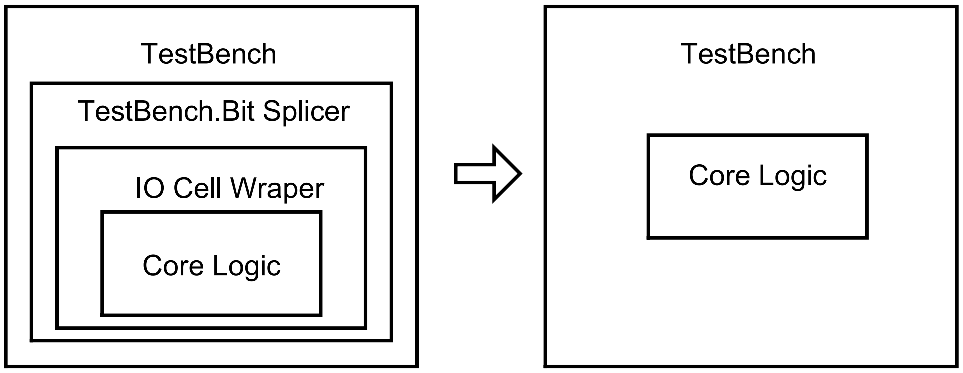

Removal of IO cell and simulation wrappers

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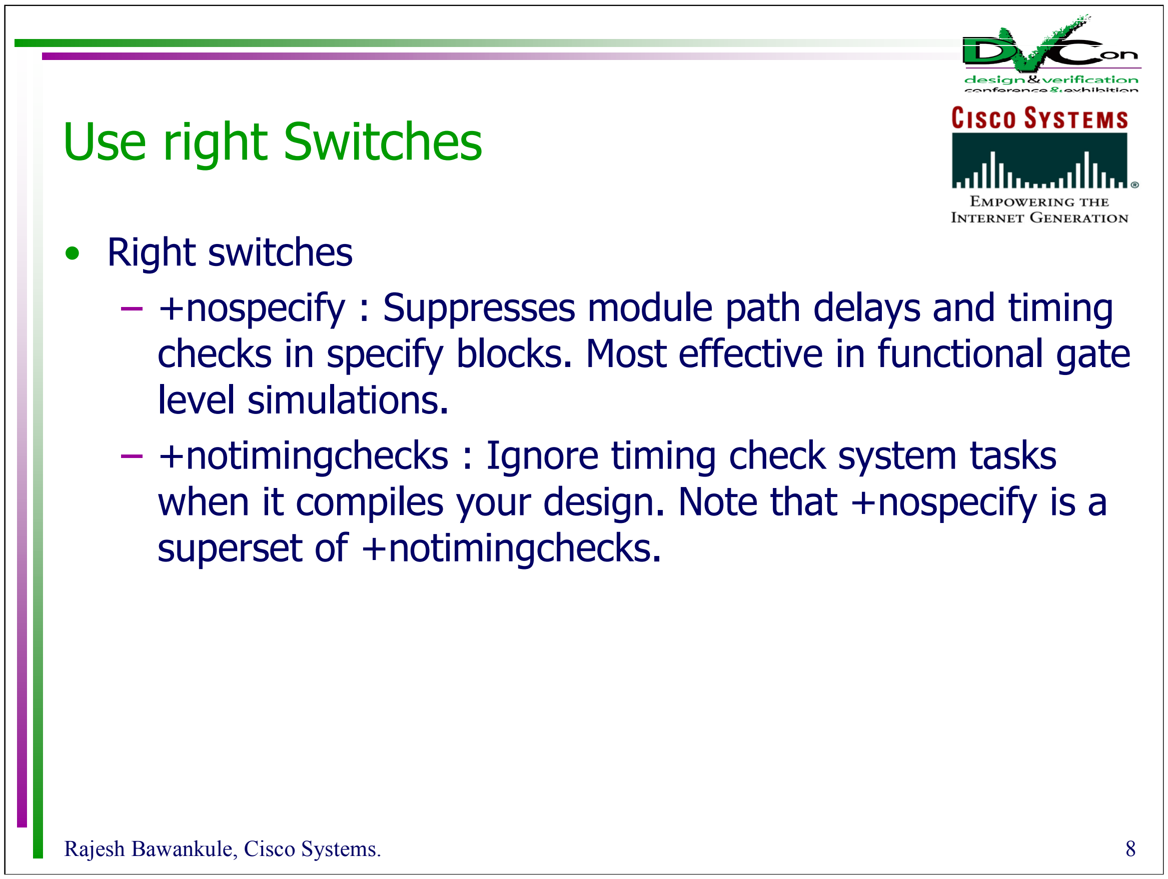
- Bit blasted buses translate to more number of simulation events and thus slow down the simulation. Carefully removing IO cell wrapper in design and Bit splicer in simulation testbench will give you tremendous boost in simulation performance.
- I have seen 25-40% saving in run times by doing this. You still need to run few key tests with IO wrappers to have confidence in your setup.



Use right Switches

- Right switches
  - +nospecify : Suppresses module path delays and timing checks in specify blocks. Most effective in functional gate level simulations.
  - +notimingchecks : Ignore timing check system tasks when it compiles your design. Note that +nospecify is a superset of +notimingchecks.

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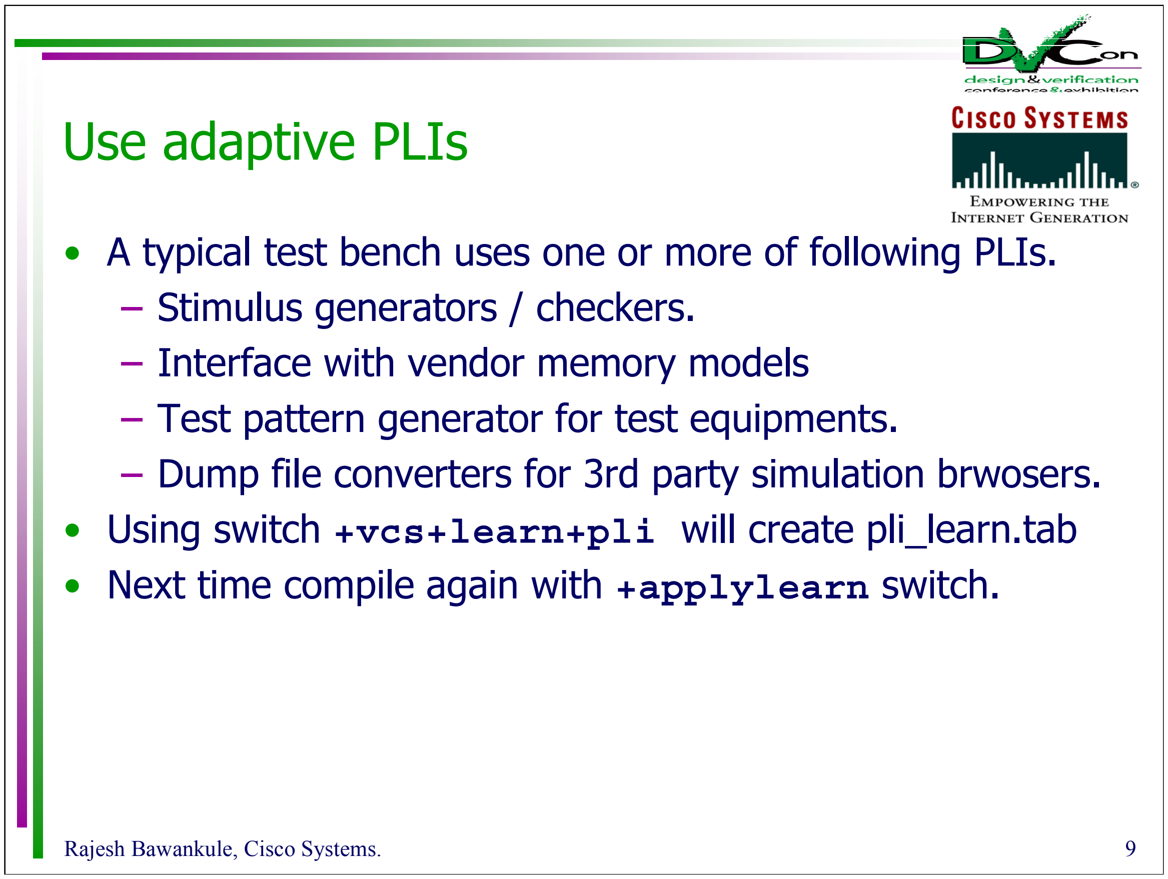
Switches that hinder performance (compile-time, runtime, and memory usage):

+cli	Turn on interactive debug on entire design
+cli+mod=#	Turn on interactive debug just for module *mod*
-line	Allow line stepping in debugger
+acc	Obsolete flag to allow global pli access
-O0	turn off optimizations
-I	Obsolete flag for interactive GUI debug
-RI	Compile and run interactive debug with VirSim GUI
-PP	Allow VirSim vcd+ binary dumping for post-processing debug
-X*	Version specific flags to work around specific bugs
+race	turn on race detection
+prof	turn on VCS profiling
-gen_c force	generation of C intermediate code instead of native object code
-gen_asm	force generation of assembly code instead of native object code
-S	the same as -gen_asm
-P	pli.tab which contains acc=rw,cbk:* globally turn on pli access
+multisource_int_delays	enables global PLI access visibility
+transport_int_delay	enables global PLI access visibility



Use adaptive PLIs

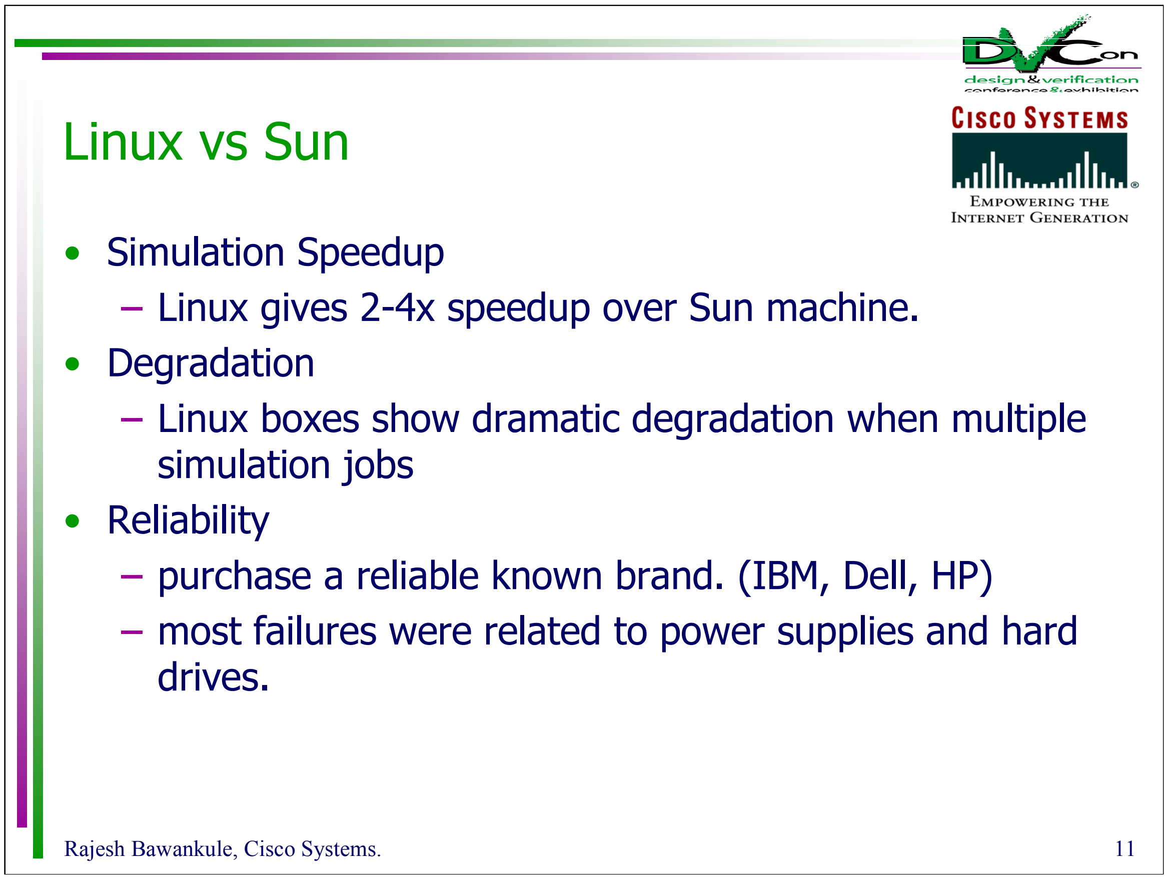
- A typical test bench uses one or more of following PLIs.
  - Stimulus generators / checkers.
  - Interface with vendor memory models
  - Test pattern generator for test equipments.
  - Dump file converters for 3rd party simulation brwosers.
- Using switch **`+vcs+learn+pli`** will create pli_learn.tab
- Next time compile again with **`+applylearn`** switch.

How to measure time

Following commands are specific to Synopsys VCS running on SunOS.

- time vcs -Mupdate –f filelist
  this will measure compile from scratch

- time ./simv
  this will measure run-time for particular simulation



Linux vs Sun

- Simulation Speedup
  - Linux gives 2-4x speedup over Sun machine.
- Degradation
  - Linux boxes show dramatic degradation when multiple simulation jobs
- Reliability
  - purchase a reliable known brand. (IBM, Dell, HP)
  - most failures were related to power supplies and hard drives.

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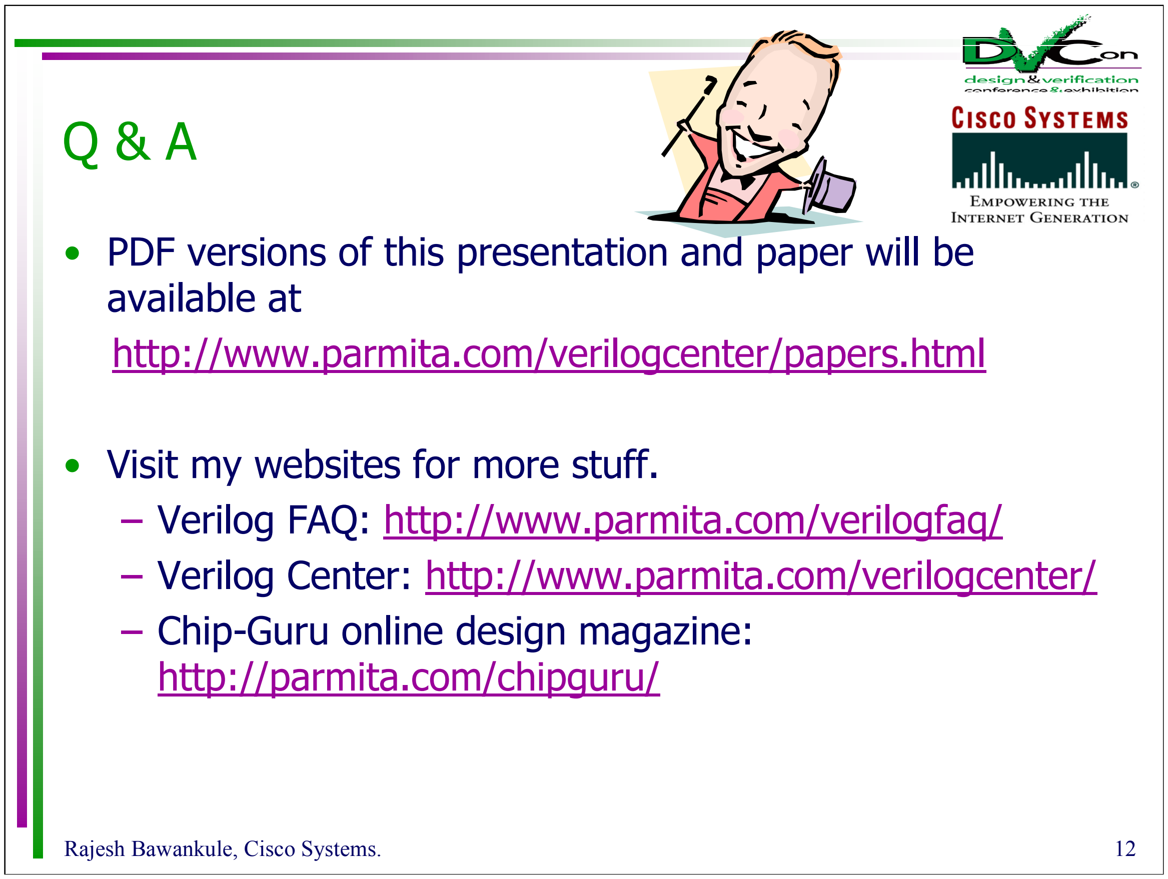

Q & A

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