[5] Hein, C., and D. Nasoff, “VHDL-based Performance Modeling and Virtual Prototyping”, *Proceedings 2nd Annual RASSP Conference*, Arlington, VA, July, 1995.

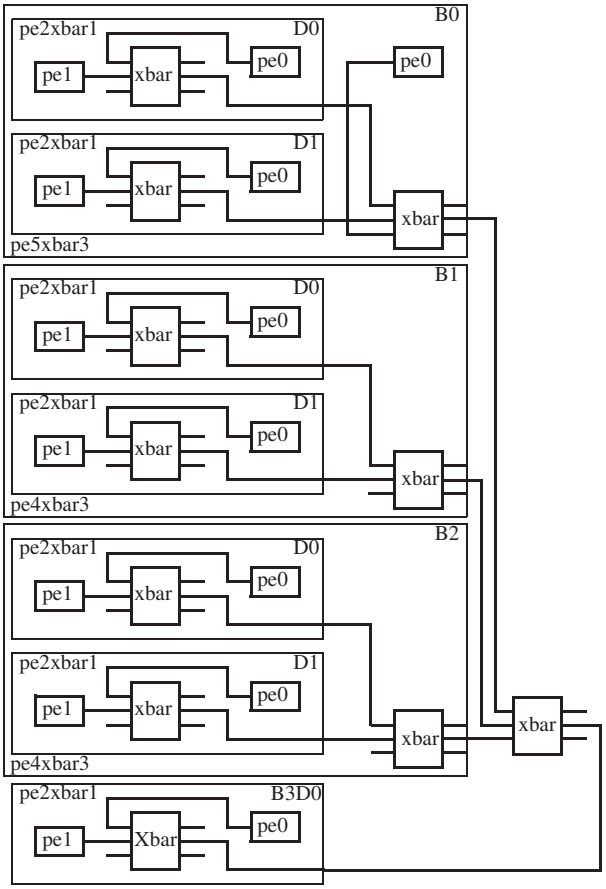

Figure 5: Mercury Raceway SAR Topology

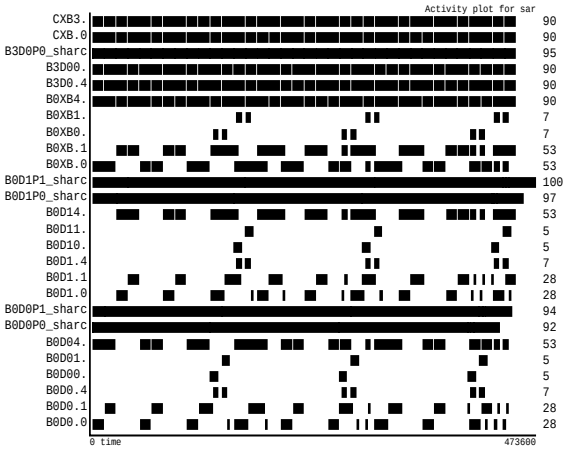

Figure 6: SAR Simulation Results

and is in nanoseconds. Objects of interest are on the vertical, and in this case show paths through the crossbars, as well as processor activity. Some of the crossbars are fairly constantly loaded, while others are lightly loaded. Numbers on the right indicate utilization of those components.

5 Summary

The SAR example was intended to demonstrate how coarse grained, abstract models could be rapidly developed using the PML. The processor model and software was developed and debugged over several weeks, and included writing some fairly portable routing routines. This processor model will be the exact same one used for the more detailed communications model. While the communications network modeled here is abstract, optimistic, and of low fidelity, the majority of the communications model required only about 4 hours to develop and debug. To be frank, several fatal bugs were found in our VHDL library, both in the processor as well as the generic modeling components, and they required many more hours to remedy. However, barring flaws in the library, the model construction and debug required roughly three weeks. The majority of the resulting model is reusable for more detailed explorations and refinement.

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