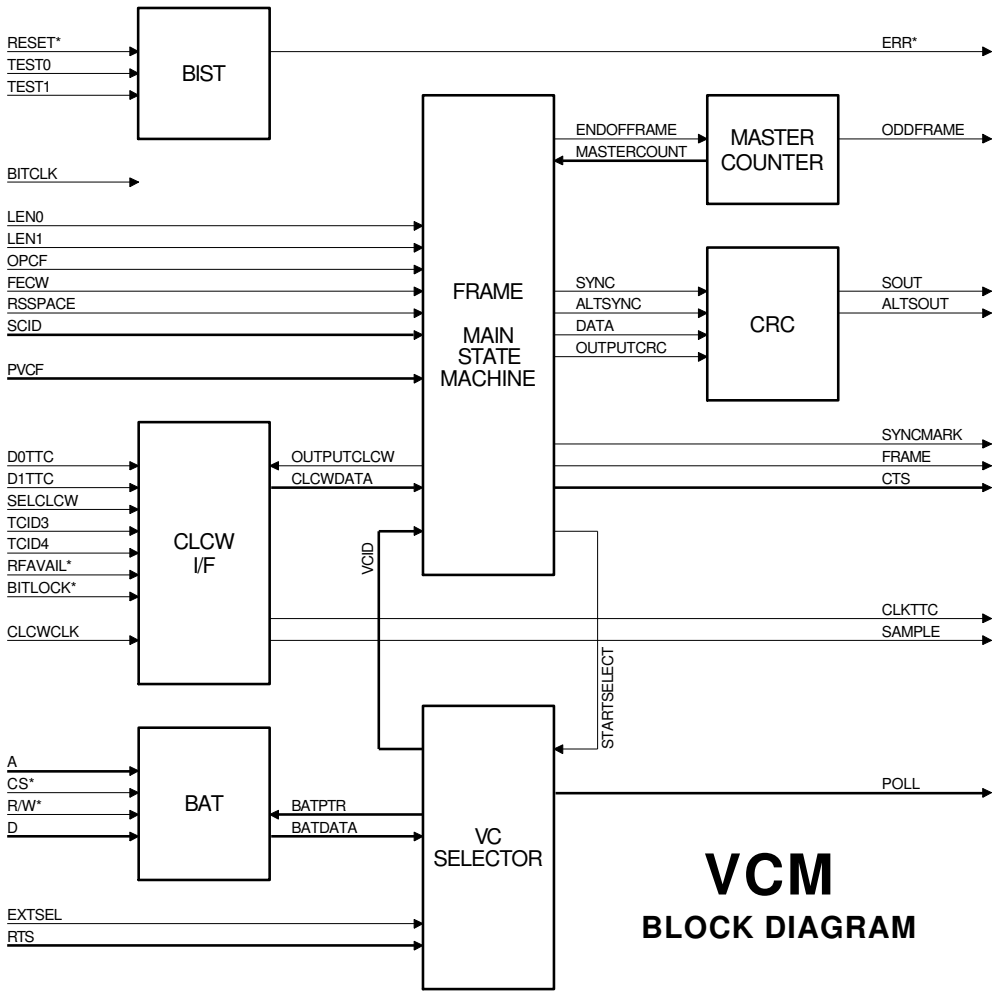
Description

The Virtual Channel Multiplexer (VCM) is a device for generating Packet Telemetry Transfer Frames. The VCM together with one Virtual Channel Assembler (VCA) per Virtual Channel, up to a maximum of eight, form a complete Transfer Frame Generator.

The VCM inputs a partial Transfer Frame from the selected VCA, attaches a Synchronisation Marker, generates parts of the Transfer Frame Header and optionally generates a Transfer Frame Trailer. If Reed-Solomon encoding is chosen, the VCM leaves a space for the codes, and generates control signals for the MA1916 encoder.

The VCM has two built-in programmable selection algorithms; Bandwidth Allocation and Priority Selection. Alternatively, other algorithms can be implemented externally.



VCM
BLOCK DIAGRAM

Features

- Fully compliant with CCSDS and ESA Packet Telemetry Standard
- Selectable frame length 223, 446, 892 or 1115 octets, with support for MA1916 Reed-Solomon encoder
- Retrieves CLCW from TC decoder
- CMOS/SOS technology; radiation hard, latch-up free, very low SEU sensitivity
- ESA/SCC part number 9544/004, to be qualified in Q2 1994
- Built-In Self Test (BIST)
- Up to 12.5 MBit/s operation

ABB HAFO AB
P.O. Box 520 S-175 26 JÄRFÄLLA SWEDEN Telephone +46 (0)8 580 24500 Telex 172 62 Telefax +46 (0)8 580 31952

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ABB HAFO AB
P.O. Box 520 S-175 26 JÄRFÄLLA SWEDEN Telephone +46 (0)8 580 24500 Telex 172 62 Telefax +46 (0)8 580 31952

1 INTRODUCTION

1.1 Reference documents

RD1 Packet Telemetry Standard, ESA PSS-04-106 Issue 1
RD2 Packet Telecommand Standard, ESA PSS-04-107 Issue 2
RD3 VCA Data Sheet, ABB HAFO

1.2 System overview

The Virtual Channel Multiplexer (VCM) is a device for generating Transfer Frames according to the ESA Packet Telemetry Standard RD1. It multiplexes serial data from one of up to eight Virtual Channel Assemblers (VCAs) as per RD3, attaches a Synchronisation Marker, generates parts of the Transfer Frame Header and optionally generates a Transfer Frame Trailer. Partial Transfer Frames are input from the selected VCA in serial form, and complete Transfer Frames with Synchronisation Markers are output as a serial bit stream. The maximum operating bit rate is 12.5 Mbit/s. All bit rates are proportional to the clock frequency used.

The length of the Transfer Frames is selectable to be 223, 446, 892 or 1115 octets. The VCM can optionally generate the 16-bit Frame Error Correction Word (FECW), which is mandatory when Reed-Solomon encoding is not used. The VCM may optionally be used with Reed-Solomon encoding and/or convolutional encoding. When using Reed-Solomon encoding the Transfer Frame lengths correspond to interleave factors of 1, 2, 4 and 5, respectively. In this mode, the VCM leaves a space for the Reed-Solomon check codes to be output from the encoder.

Each of the eight serial VCA interfaces is intended to be connected to a VCA as defined in RD3. The serial output provides signals for directly interfacing with the radiation hard MA1916 Reed-Solomon encoder from GEC Plessey Semiconductors, if Reed-Solomon encoding is used.

The VCM features two built-in algorithms for selecting which Virtual Channel to output the next Transfer Frame:

- Bandwidth Allocation guarantees a minimum bandwidth for each Virtual Channel. In this mode, the VCM uses adaptive frame ordering, in order to utilize the available bandwidth as efficiently as possible.

- Priority Selection; the VCM selects the highest priority Virtual Channel that can produce a normal Transfer Frame. The priority of each Virtual Channel is programmable.

Alternatively, if the built-in algorithms are not suitable, a user-defined algorithm can be implemented externally.

The VCM has a 3-bit parallel bus for programming the Bandwidth Allocation Table, which can be connected to any CPU bus.

The VCM includes a TTC-B-01 interface for retrieving part of the Command Link Control Word (CLCW) directly from one or two Packet Telecommand Decoders according to RD2. The VCM can toggle between the two decoders as CLCW source. The remaining parts of the CLCW are either input through pins on the VCM or are fixed.

The VCM operating mode is determined by input pins instead of using a mode register, which would have been SEU sensitive. The VCM features Built-In Self Test (BIST), that can be automatically activated after reset.

Note: the VCM is designed to be used on the same circuit board as the VCAs and a Reed-Solomon encoder, forming a Transfer Frame Generator.

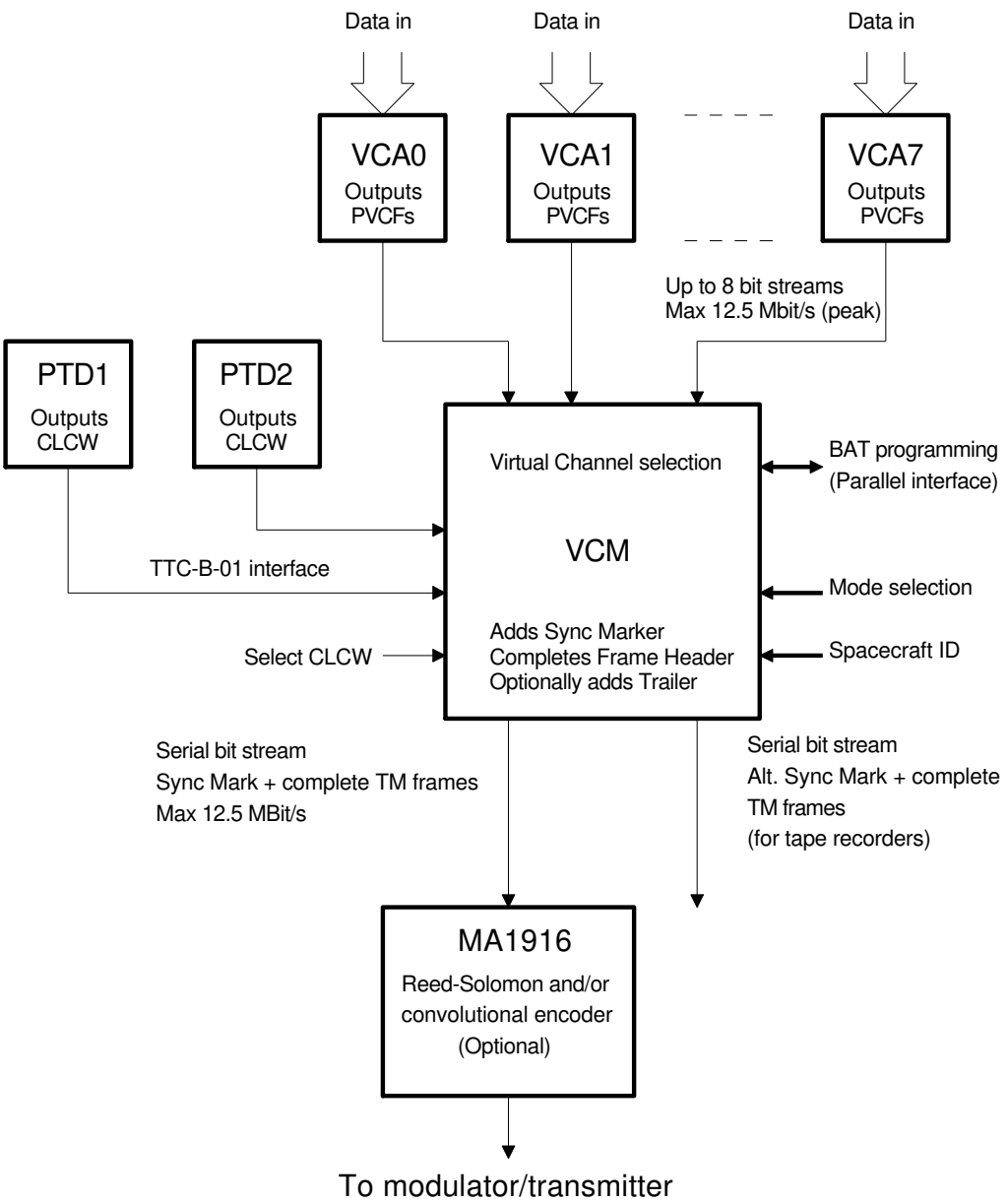

Figure 1: Typical environment for the Virtual Channel Multiplexer

2 TRANSFER FRAME FORMAT

The VCM handles frames with a format according to RD1. Transfer Frame lengths of 223, 446, 892 or 1115 octets are selectable, allowing the frames to be usable both with and without Reed-Solomon encoding. The Command Link Control Word (CLCW) and the Frame Error Correction Word (FECW) fields in the trailer can be independently included or omitted. The most common setting is a length of 1115 octets using Reed-Solomon encoding, with both the FECW and OPCF present.

The VCM outputs Transfer Frames with the following structure:

<table>
<tr><td colspan="5">Transfer Frame</td></tr>
<tr><td>By VCM</td><td colspan="3">Partial Virtual Channel Frame, by VCA</td><td>By VCM</td></tr>
<tr><td colspan="2">Transfer Frame Header</td><td>Transfer Frame Data Field</td><td rowspan="2">Transfer Frame Trailer (optional)</td></tr>
<tr><td colspan="2">Primary</td><td>Secondary (optional)</td><td>ket | Packet | Packet | Packet | Pa</td></tr>
<tr><td>3 oct.</td><td>3 oct.</td><td>0/4 octets</td><td></td><td>0/2/4/6 octets</td></tr>
<tr><td colspan="5">223/446/982/1115 octets</td></tr>
</table>

Note that the Partial Virtual Channel Frame (PVCF) is a result of the split of the functionality between the VCA and the VCM. The PVCF is only an internal structure, not defined in the Packet Telemetry Standard, and can be disregarded from the system point of view.

Transfer Frame Primary Header structure:

<table>
<tr><td colspan="6">Transfer Frame Primary Header</td></tr>
<tr><td colspan="4">Generated by the VCM</td><td colspan="2">Generated by the VCA</td></tr>
<tr><td colspan="4">Frame Identification</td><td rowspan="2">Master Channel Frame Count</td><td rowspan="2">Virtual Channel Frame Count</td><td rowspan="2">Frame Data Field Status</td></tr>
<tr><td>Version = ’00’</td><td>S/C Id</td><td>VC Id</td><td>OPCF Flag</td></tr>
<tr><td>2 bits</td><td>10 bits</td><td>3 bits</td><td>1 bit</td><td>8 bits</td><td>8 bits</td><td>16 bits</td></tr>
<tr><td colspan="4">2 octets</td><td>1 octet</td><td>1 octet</td><td>1 octet</td></tr>
</table>

Transfer Frame Trailer structure, generated by the VCM:

<table>
<tr><td colspan="2">Transfer Frame Trailer</td></tr>
<tr><td>Operational Control Field (opt.)</td><td>Frame Error Control Word (opt.)</td></tr>
<tr><td>0/4 octets</td><td>0/4 octets</td></tr>
</table>

Output bit stream from the VCM, no Reed-Solomon encoding:

ansfer Frame	Att. Sync. Marker	Transfer Frame	Att. Sync. Marker	Transfer Fra
	4 octets	223/446/892/1115 octets		

Output bit stream from the VCM when using a Reed-Solomon encoder:

Logic 0	Att. Sync. Marker	Transfer Frame	Logic 0	Att. S
	4 octets	223/446/892/1115 octets	32/64/128/160 octets	

The space with logic 0 leaves room for the Reed-Solomon check codes to be inserted by the Reed-Solomon encoder.

Throughout this document bit 0 is the most significant bit and is input/output first when transferred as a serial bit stream.

3 FUNCTIONAL SPECIFICATION

3.1 Summary of operation

- After reset, the VCM performs a self-test (optionally) and then automatically starts outputting Transfer Frames continuously:
  - Generates and outputs the 32 bit Attached Synchronisation Marker.
  - Generates and outputs the Frame Identification and the Master Channel Frame Count fields of the Transfer Frame Primary Header.
  - Feeds through the Partial Virtual Channel Frame from the selected VCA.
  - Optionally generates and outputs the Transfer Frame Trailer.
  - Optionally leaves space for the Reed-Solomon check codes, and generates the control signals for the MA1916 Reed-Solomon encoder.

- If the built-in selection algorithms are used, the VCM selects which VCA is to output the next Partial Virtual Channel Frame (PVCF). If no PVCF was found to be available, the VCM demands the VCA for Virtual Channel 7 to produce a PVCF, normally resulting in an Idle Transfer Frame.

  If external selection is employed, the VCA specified by 3 input pins is demanded to provide a PVCF. If the selected VCA cannot provide a normal PVCF, an idle PVCF is sent, resulting in an Idle Transfer Frame being output for that Virtual Channel.

- During operation, the bandwidth allocation (or the priority order) for the selection of the next Virtual Channel to be output may be reprogrammed.

- The VCM retrieves part of the Command Link Control Word (CLCW) from the Packet Telecommand Decoder, using the TTC-B-01 interface. The retrieved data will form part of the OPCF in the trailer.

3.2 Functions not included in the VCM

The VCM does not produce Idle Transfer Frames. Instead, if the selected VCA does not have a complete PVCF available, it will output an idle PVCF, resulting in an Idle Transfer Frame being output from the VCM.

The VCM does not generate or insert the Reed-Solomon check block, or perform any interleaving functions. This is handled by a Reed-Solomon encoder such as the MA1916. The same applies for convolutional encoding.

3.3 VCA/VCM interface

The VCM has two inputs and two outputs for each of the eight VCAs that can be connected. One VCA is required per Virtual Channel. The inputs are Ready To Send (RTS0 to RTS7) and Partial Virtual Channel Frame (PVCF0 to PVCF7). The outputs are Clear To Send (CTS0 to CTS7) and Device Polled (POLL0 to POLL7). The POLL signals are described in section 3.6. The VCM operates on the falling BITCLK edge, whereas the VCA operates on the rising BITCLK edge, to avoid skew problems.

When the VCA is ready to transfer a complete PVCF, it asserts its RTS signal. If the built-in selection algorithms are used, the VCM selects one of the VCAs whose RTS input is asserted. With external selection the VCA indicated by RTS0 to RTS2 is selected.

The VCM asserts the CTS output corresponding to the selected VCA. Four BITCLK cycles later, the VCM samples the data from the VCA present on the corresponding PVCF input, to be output at the SOUT and ALTSOUT outputs. A new bit value is sampled every BITCLK cycle until the complete PVCF has been fed through. The CTS signal remains asserted for 461 BITCLK cycles.

A schematic view of the interface as seen by the VCM is presented in figure 2. In this example one of the internal selection algorithms is used.

The size of the PVCF depends on both the length of the Transfer Frame, defined by the LEN0 and LEN1 inputs, and whether the Operational Control Field (OPCF) and/or the Frame Error Correction Word (FECW) shall be generated, as determined by the OPCF and FECW inputs. The PVCF lengths are:

Transfer Frame length	LEN0	LEN1	OPCF	FECW	PVCF length
223 octets	0	0	0	0	220 octets
223 octets	0	0	0	1	218 octets
223 octets	0	0	1	0	216 octets
223 octets	0	0	1	1	214 octets
446 octets	0	1	0	0	443 octets
446 octets	0	1	0	1	441 octets
446 octets	0	1	1	0	439 octets
446 octets	0	1	1	1	437 octets
892 octets	1	0	0	0	889 octets
892 octets	1	0	0	1	887 octets
892 octets	1	0	1	0	885 octets
892 octets	1	0	1	1	883 octets
1115 octets	1	1	0	0	1112 octets
1115 octets	1	1	0	1	1110 octets
1115 octets	1	1	1	0	1108 octets
1115 octets	1	1	1	1	1106 octets

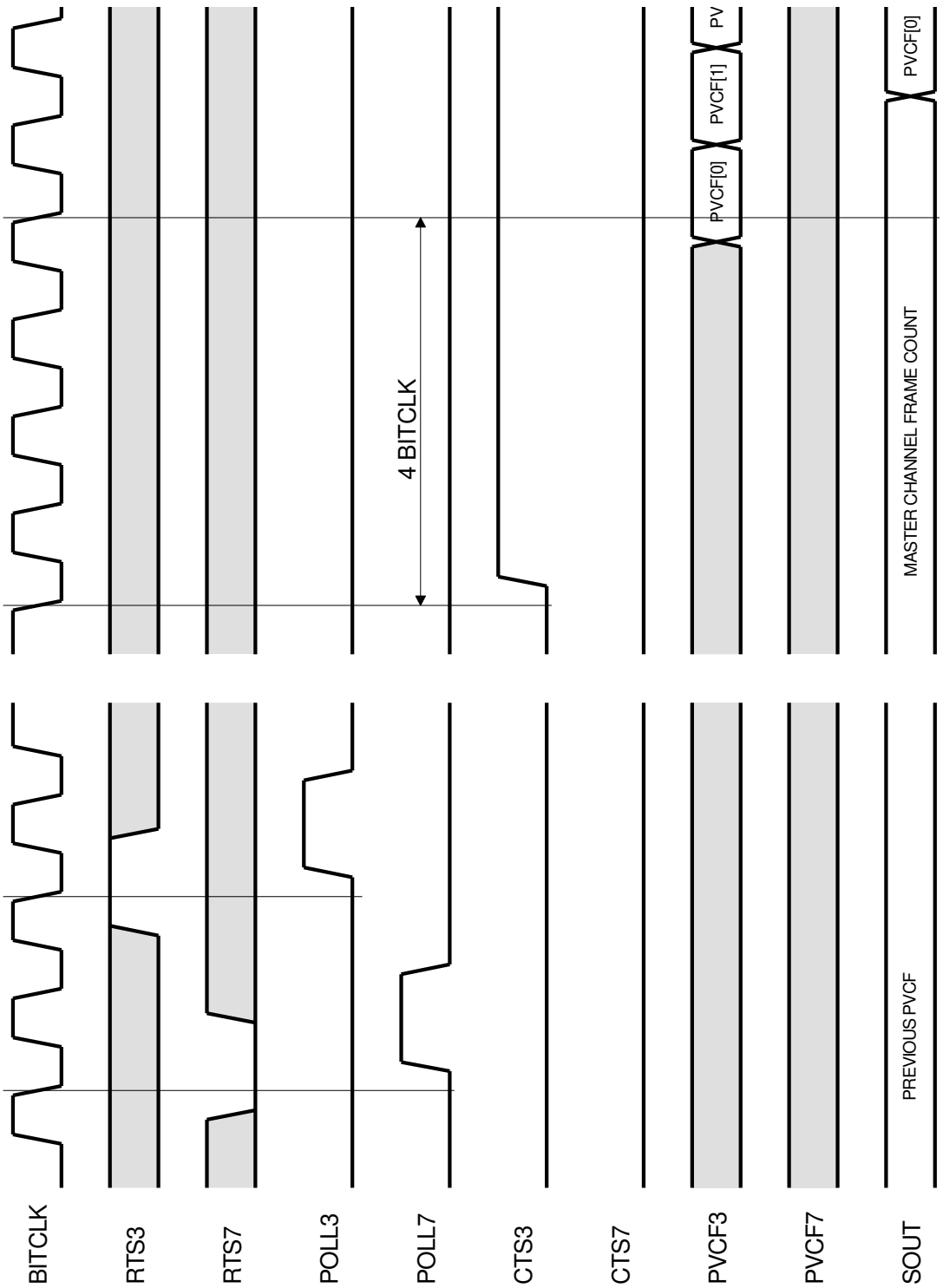

Figure 2: VCA/VCM interface

3.4 Bandwidth Allocation Table interface

The Bandwidth Allocation Table (BAT) is used by the built-in selection algorithms, described in section 3.6.

Data can be written to the BAT using a 3-bit parallel bus. The data consists of 32 entries of three bits each. Which entry is read or written is selected by the 5-bit address bus A0 to A4. Note: D0 and A0 are the most significant bits of the data bus and the address bus, respectively.

The BAT interface is asynchronous. It is possible to both read and write data while the VCM is operating. CS* must be de-asserted for a minimum of four BITCLK cycles after a write, to allow for internal updating of the BAT. The interface is shown in figure 3.

After reset, the BAT contains 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2 ..., so that all Virtual Channels will have an equal bandwidth allocated. In the case of Priority Selection, this will mean that Virtual Channel 0 then has the highest priority, and Virtual Channel 7 the lowest.

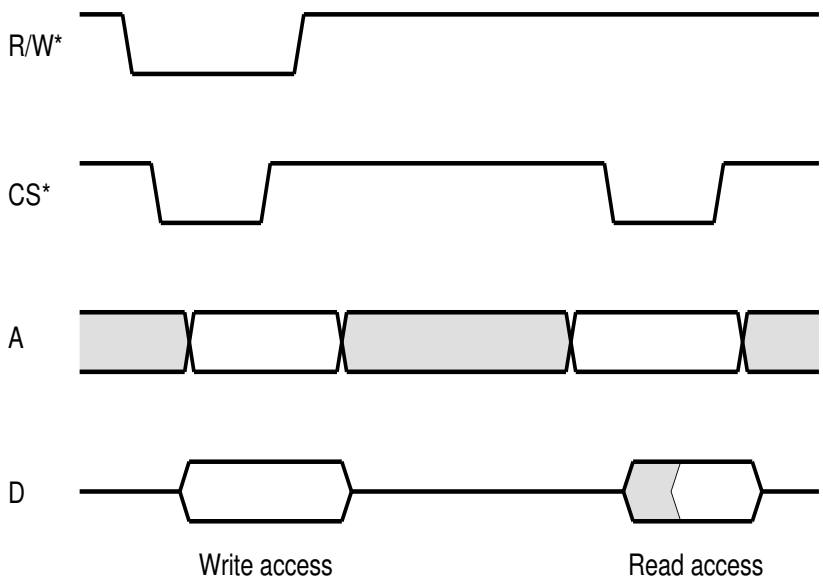

Figure 3: BAT interface

3.5 CLCW interface

The 32-bit Command Link Control Word (CLCW), as specified in RD2, consists of, in output order:

- Control Word Type (bit 0) is 0.
- CLCW Version Number (bits 1 - 2) is 00.
- Status Field (bits 3 - 5) is 000.
- COP in Effect (bits 6 - 7) is 01.
- Virtual Channel Identifier (bits 8 - 13) describes which Packet TC decoder is used for the CLCW. For the VCM, bits 8 - 10 are fixed to 000, bit 11 gets its value from the TCID3 input, bit 12 gets its value from the TCID4 input, and bit 13 gets its value from the SELCLCW input (also used for selecting the CLCW source).
- Reserved Field (bits 14 - 15) is 00.
- No RF Available Flag (bit 16) has the same value as the RFAVAIL* input.
- No Bit Lock Flag (bit 17) has the same value as the BITLOCK* input.
- Bits 18 - 31 are retrieved from the Packet TC decoder using a TTC-B-01 interface, as shown in figure 4. This part of the CLCW is normally retrieved once per transmitted frame, depending on the CLCWCLK frequency. Bit 18 gets its value from bit 2 of the retrieved word, and bit 31 gets its value from bit 15 of the retrieved word (the LSB).

The VCM generates the CLKTTC and SAMPLE output signals for controlling the CLCW interface, and inputs the D0TTC or the D1TTC signal from the Packet TC decoder. The retrieval starts at the same time the frame starts to be output. All signals related to the CLCW interface are proportional to the CLCWCLK frequency. The transfer rate equals CLCWCLK divided by 80, e.g. if CLCWCLK is 10 MHz the CLCW interface is operating at 125 kbit/s. CLCWCLK is normally connected to the same clock as BITCLK. However, in the case another frequency is desired, a separate clock signal can be connected to CLCWCLK as explained in appendix B.

The interface has been designed to retrieve one CLCW per Transfer Frame generated, regardless of the frame length, when CLCWCLK is connected to the same clock as BITCLK. The interface allows direct connection to a Packet TC decoder chip without additional components. Alternatively, another electrical interface can be designed using external components.

Since the SELCLCW, TCID3 and TCID4 inputs indicate which Packet TC decoder the CLCW originates from, they are latched on the falling SAMPLE edge, to not change while the CLCW is acquired. These three latched signals, together with the 14 bits retrieved from the TTC-B-01 interface, are transferred to the OPCF register on the rising SAMPLE edge.

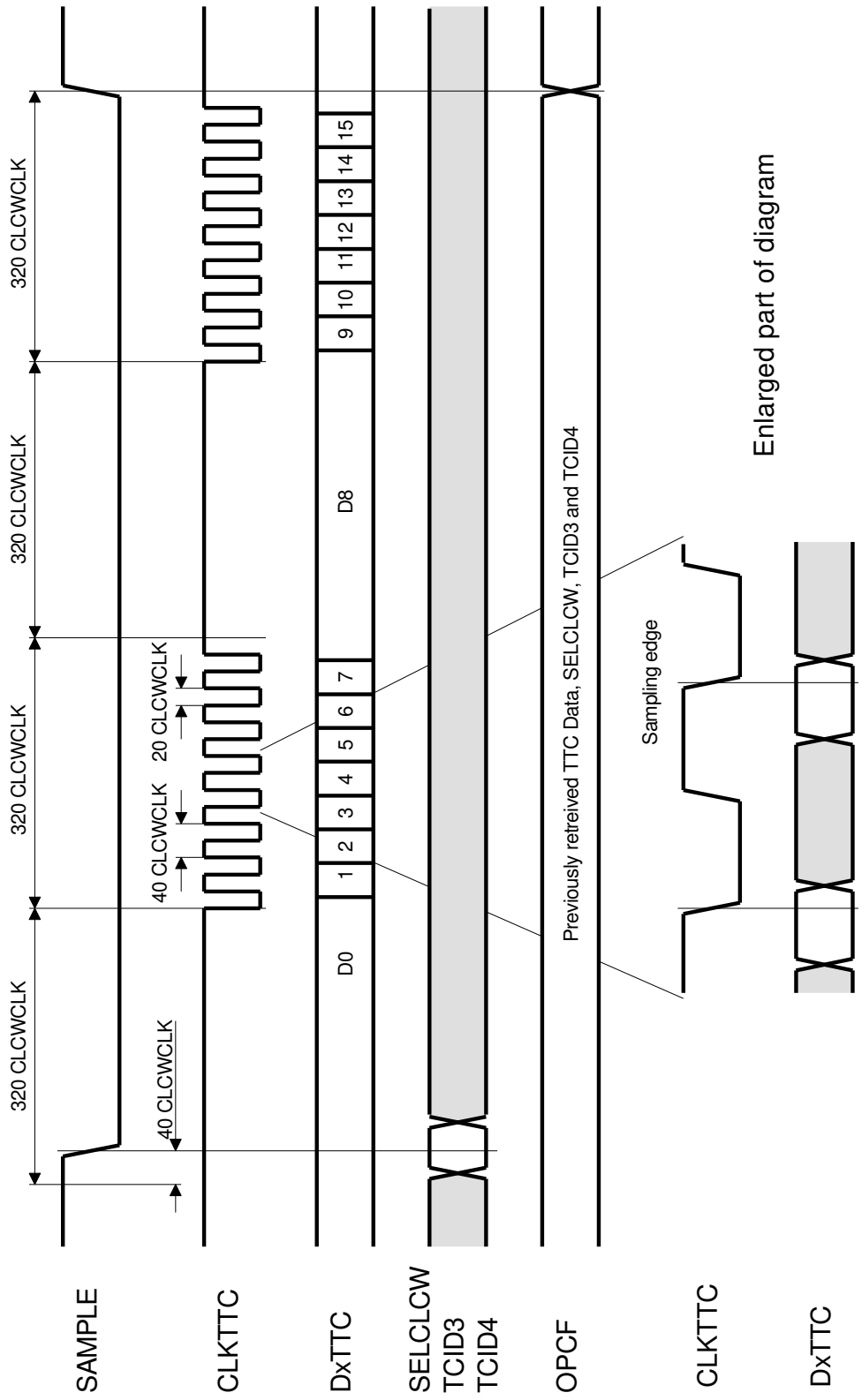

Figure 4: TTC-B-01 interface for the CLCW

The VCM provides a mechanism for multiplexing the CLCW from two Packet TC decoders. Which data input is used is determined by the SELCLCW signal, latched as described above. D1TTC is used when the latched SELCLCW = 1, otherwise D0TTC is used. If three to eight Packet TC decoders are used, they can be multiplexed externally, the source being indicated by the TCID3 and TCID4 inputs.

The ODDFRAME output can be connected to the SELCLCW input to automatically toggle between the two Packet TC decoders as CLCW source (provided that an odd number of Transfer Frames are output per CLCW acquisition). When CLCWCLK is connected to BITCLK, each Transfer Frame with an even Master Channel Frame Count will have a CLCW retrieved from the D0TTC and D1TTC inputs for odd Transfer Frames.

3.6 Selection of next Virtual Channel to output a Transfer Frame

The VCM features two built-in algorithms for selecting the next Virtual Channel to output a Transfer Frame: Bandwidth Allocation and Priority Selection. Alternatively, a user-defined algorithm can be implemented externally if the built-in algorithms are not suitable. Examples of different selection algorithms can be found in appendix A.

3.6.1 Bandwidth Allocation

This mode is enabled when the EXTSEL input is logic 0. In this mode the VCM uses adaptive frame ordering, as described in appendix A. The Bandwidth Allocation Table (BAT) contains 32 internal 3-bit registers whose value (0 to 7) indicates the number of the Virtual Channel to be considered.

While outputting a Transfer Frame the VCM scans the BAT for the next ready frame to be output in a round-robin fashion. The algorithm selects the next entry in the BAT which points to a VCA that has asserted its corresponding RTS signal. If a Virtual Channel does not have an entry in the BAT that points to it, no Transfer Frames from that Virtual Channel will be output, even if no other Transfer Frames are available.

The round-robin scanning continues until one asserted RTS has been found, or all entries in the BAT have been examined (33 entries are examined). If none of the VCAs pointed to by the BAT entries had asserted their RTS signal, the VCM asserts the CTS7 output, requesting the VCA for Virtual Channel 7 to produce a PVCF. VCA 7 then produces an idle PVCF, resulting in an Idle Transfer Frame being output from the VCM (if VCA 7 is also used for sending normal data, and enough data have become available, a normal PVCF is supplied instead).

This function can be used to send low-priority data instead of idle frames; if data are fed to VCA 7, but no entry in the BAT points to it, Virtual Channel 7 will have the lowest priority; all other Virtual Channels have their guaranteed Bandwidth, but VCA 7 will use the spare bandwidth when no other VCA can provide a normal PVCF.

The selection starts when approximately 80 % of the previous frame has been output to allow the algorithm to complete before the next frame. The exact figures are: 1536 BITCLK cycles after the first bit of the Synchronisation Marker for a frame length of 223 octets; 3072 cycles for 446 octets; 6144 cycles for 892 octets; and 8192 cycles for 1115 octets. Since the selection occurs while the previous Transfer Frame is being output, the first frame after reset has been chosen to be from VCA 7.

For each entry in the BAT that is scanned the VCM asserts the corresponding POLL output for the duration of one BITCLK cycle. Consequently a VCA may receive between 0 and 33 polls for each Transfer Frame being output, depending on the BAT programming. The POLL signal may be used by a VCA to recognize that it has been considered for outputting a PVCF.

3.6.2 Priority Selection

This mode is enabled when the SYNCMARK output is connected to the EXTSEL input. On the falling SYNCMARK edge the BAT pointer is reset to restart at the first entry in the BAT (address 0). Since this occurs after each selection (Transfer Frame), the result will effectively be a priority selection. Except for the repeated resetting the selection process works exactly as in the case of Bandwidth Allocation.

3.6.3 External Selection

This mode is enabled when EXTSEL is connected to logic 1. In this mode the selection has to be external and should be provided through RTS0 to RTS2. RTS0 is the most significant bit. The value at RTS0 to RTS2 is sampled on the rising SYNCMARK edge. The RTS3 to RTS7 signals are not used but should be connected to a defined logic level.

If the selected VCA has a PVCF available it will provide a normal PVCF, otherwise an idle PVCF is sent resulting in an Idle Transfer Frame being output for that Virtual Channel. The selection also applies for the first Transfer Frame after reset, which normally will be an Idle Transfer Frame since the VCAs have not received enough data.

Note: in this mode the selection algorithm still operates internally, toggling the POLL outputs according to the BAT programming.

3.7 Attached Synchronization Marker

Before outputting the Transfer Frame the VCM generates and sends the 32 bit Attached Synchronisation Marker. The VCM has two outputs, SOUT and ALTSOUT, which continuously output the same Transfer Frames, but with different Synchronisation Markers. For the SOUT output, the hexadecimal value of the Attached Synchronisation Marker is 1ACFFC1D.

For applications that use a tape recorder that plays back a recorded data stream in forward order, the ALTSOUT output can be used instead of the SOUT output for the data to be recorded. This pin outputs the hexadecimal value 352EF853 for the Attached Synchronization Marker, but is otherwise identical to the SOUT output.

If Reed-Solomon encoding is used a space will be present on both the SOUT and ALTSOUT outputs. If only one Reed-Solomon encoder is used both for the SOUT and ALTSOUT outputs (e.g. for error correction for the tape recorder), the synchronization marker, or the check codes, have to be multiplexed externally.

3.8 Transfer Frame Primary Header

The fields in the first three octets of the Primary Header generated by the VCM are, in the order they are output:

- Version number, always 00.
- Spacecraft Identifier (S/C Id), has the same value as inputs SCID0 to SCID9.
- Virtual Channel Identifier (VC Id) is the number of the Virtual Channel currently being output.
- Operational Control Field Flag (OPCF Flag), indicates whether the Operational Control Field is present in the Trailer or not. This flag has the same value as the input pin OPCF.
- Master Channel Frame Count, retrieved from the Master Frame Counter. This 8-bit counter is incremented by one for each frame that is output.

3.9 Transfer Frame Trailer

The Trailer consists of two optional fields:

- The four octet Operational Control Field (OPCF) is present when the input OPCF = 1. This field contains the Command Link Control Word (CLCW), updated on the rising SAMPLE edge, as described in section 3.5.

- The two octet Frame Error Control Word (FECW) is present when the input FECW = 1. It consists of the CRC checksum over the whole Transfer Frame, excluding the FECW and the Synchronization Marker, using the generator polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$. The shift register is initialized to 'all ones' before each frame.

3.10 Space for Reed-Solomon check codes

A space for Reed-Solomon check codes between the Transfer Frames can be selected with the RSSPACE input. When RSSPACE = 1, the space is present and both the SOUT and ALTSOUT outputs are logic 0 after the Transfer Frame has been output. The space is output after normal as well as after Idle Transfer Frames. The length of this space depends on the inputs LEN0 and LEN1 as described in section 4.5.1.

3.11 Idle Transfer Frames

If the VCA for which CTS is asserted has a complete PVCF available it will provide a normal PVCF, otherwise an idle PVCF will be generated, resulting in an Idle Transfer Frame being output for that Virtual Channel.

All fields generated by the VCM are the same as for a normal frame. The VCA will generate the correct flags and counter values, and provide an adequate fill pattern for the data field.

3.12 Transfer Frame outputs

The Attached Synchronisation Marker, the complete Transfer Frames and the optional space for Reed-Solomon check codes are output through the SOUT and ALTSOUT outputs.

The VCM is designed to suit the interface of the MA1916 Reed-Solomon encoder, if Reed-Solomon encoding is used. The output signal FRAME is intended to be connected to the SMC input of the MA1916 to control the generation and output of the check codes. FRAME is asserted when the first part of the transfer frame is being output. It is de-asserted when the last bit of the Transfer Frame has been output. It also is de-asserted when the Attached Synchronisation Marker is being output, so that it is not included in the generation of the check symbols.

3.13 Test

The VCM features Built-In Self Test (BIST) with a fault coverage of 92 %. The BIST runs for 4997 BITCLK cycles after RESET* has been released. The BIST result does not depend on the state of any of the input pins. The BIST can be disabled by connecting the TEST0 input to logic 1; after releasing RESET* the VCM will be reset but no BIST will be performed.

If an error is detected by the BIST, the ERR* output remains asserted (ERR* = 0), until the next reset occurs. The VCM will try to continue to operate in normal mode. If no internal error was detected the ERR* output is de-asserted and the VCM starts working in normal mode.

When RESET* is asserted and during BIST, the CLKTTC and SAMPLE outputs are driven to logic 1, the D data bus is tristated, and all other outputs set to logic 0 so as not to trigger connected devices.

The production test for the VCM has a fault coverage of 99 %, and is performed at a BITCLK frequency of 10 MHz. The TEST1 input is used for the production test and shall be tied to logic 0 during normal operation.

The fault coverage figures are based on stuck-at-0/1 faults at the gate level, faulting all nets (gate outputs).

3.14 State after reset

After reset, or after reset and the completion of BIST, the VCM is initialized as follows:

- The BAT contains 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2 ..., so that all Virtual Channels will have an equal bandwidth allocated. In the case of Priority Selection, this will mean that Virtual Channel 0 then has the highest priority and Virtual Channel 7 the lowest.

- The Master Channel Frame Count field has the value 0. The ODDFRAME signal has the value 0. Finally, bits 18 - 31 of the CLCW are set to 0, though normally data will be retrieved from the Packet TC decoder before the CLCW is output.

- The VCM starts outputting the Synchronization Marker of the first Transfer Frame after reset, which is normally an Idle Transfer Frame since the VCAs have not received enough data. If internal selection is used this frame will come from VCA 7, otherwise it will come from the VCA defined by the external selection.

The selection also applies for the first Transfer Frame after reset, which normally will be idle, since the VCAs have not received enough data.

4 INTERFACE AND SIGNAL DESCRIPTION

The VCM has 51 input signals, 24 output signals and 3 bidirectional signals. Together with 6 power supply pins, this gives a total pin count of 84. The character * is used to indicate an active low signal.

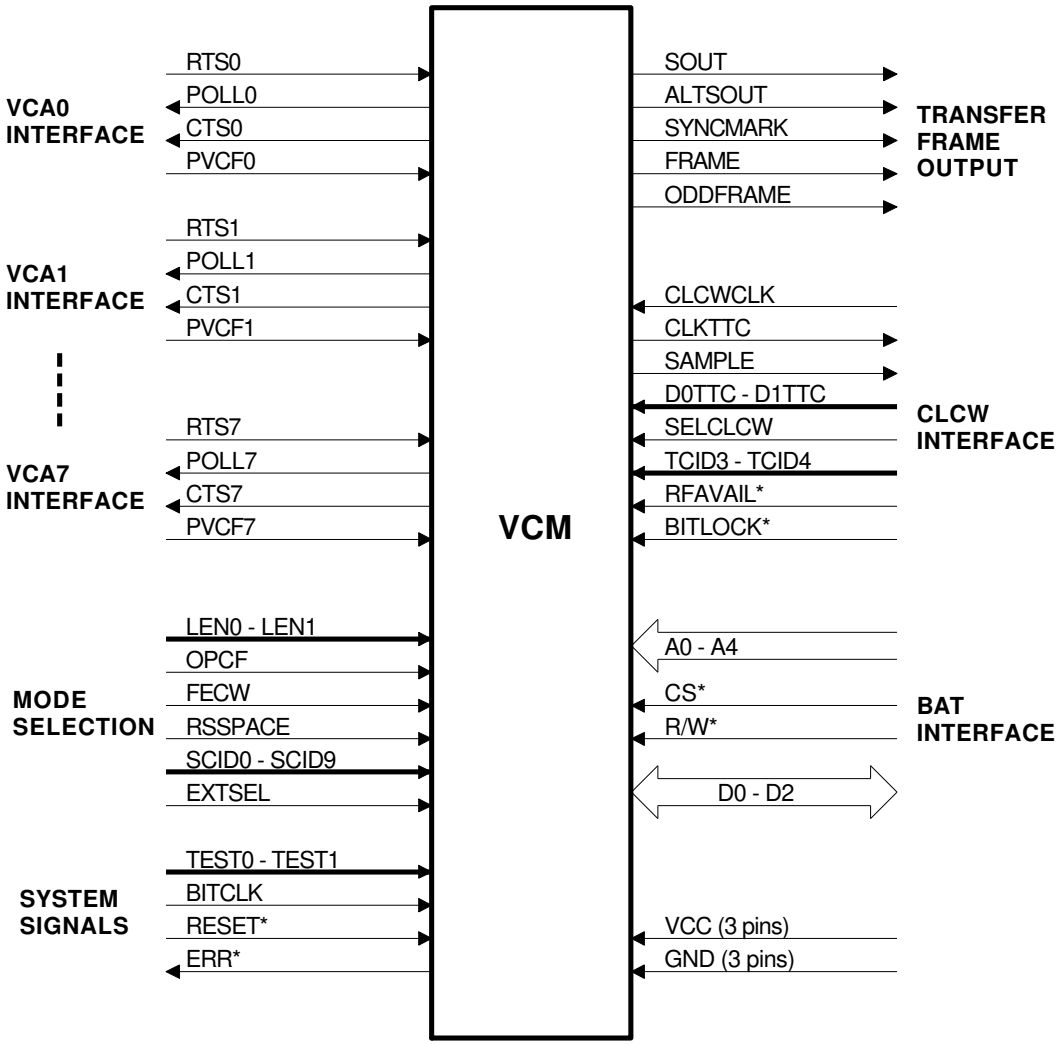

Figure 5: Signal overview

4.1 VCA interface, 32 pins

4.1.1 RTS0 to RTS7: VCA Ready To Send (I)

Each of these eight CMOS inputs indicates when the corresponding VCA has a PVCF ready. The PVCF is available when the corresponding RTS = 1. When the selection of which Virtual Channel is to output the next PVCF is made externally, the value is input from RTS0 to RTS2, with RTS0 being the most significant bit. RTS shall be stable on the falling BITCLK edge.

4.1.2 POLL0 to POLL7: VCA Polled (O)

Each of these eight outputs indicates that the VCM built-in selection algorithms considered the corresponding VCA to output the next frame. Each time an RTS input is sensed, the corresponding POLL output is asserted for one BITCLK cycle. POLL changes state on the falling BITCLK edge.

4.1.3 CTS0 to CTS7: VCA Clear To Send (O)

Each of these eight outputs indicates that the corresponding VCA should output a complete PVCF, when the associated CTS = 1. CTS changes state on the falling BITCLK edge.

4.1.4 PVCF0 to PVCF7: VCA Serial PVCF Input (I)

Each of these eight serial CMOS inputs is intended to receive a PVCF from the VCA. The first bit (the most significant bit of the Virtual Channel Frame Counter) of the PVCF shall be present at the corresponding PVCF input. A new bit shall be present for each following BITCLK cycle until the complete PVCF has been input. The data on the PVCF input are fed to the SOUT and ALTSOUT outputs without processing. PVCF shall be stable on the falling BITCLK edge.

4.2 Parallel BAT interface, 10 pins

4.2.1 A0 to A4: Address bus for the BAT (I)

These are asynchronous TTL inputs, A0 is the most significant bit (Example: A0 = A1 = A2 = A3 = 0 and A4 = 1 for BAT entry number 1). This 5-bit address bus selects which entry in the BAT is accessed with the data bus.

4.2.2 CS*: Chip Select (I)

This active low TTL input may be asynchronous. When CS* = 0 it enables the parallel interface of the VCM and indicates that a valid address and R/W* signal (and also data for a write access) are available. For a write access the address and data bus are latched on the rising CS* edge. The BAT should not be accessed during four BITCLK cycles after a write access, to allow the BAT to be updated internally.

4.2.3 R/W*: Read/Write control (I)

This TTL input may be asynchronous but shall be stable while CS* is asserted. It defines whether a read (R/W* = 1) or a write (R/W* = 0) operation is performed.

4.2.4 D0 to D2: Data bus for the BAT (I/O)

These are bidirectional TTL signals, D0 is the most significant bit (Example: D0 = D1 = 0 and D2 = 1 represents the value 1). D may be asynchronous.

The BAT can be reprogrammed concurrently with the selection of the next Virtual channel to output.

4.3 CLCW interface, 10 pins

The CLKTTC, SAMPLE, D0TTC and D1TTC signals are based on the TTC-B-01 specification for 16 bit transfers.

4.3.1 CLCWCLK: Clock for generating CLCW control signals (I)

This separate clock CMOS input is used for the generation of all TTC-B-01 signals and allows for implementing an arbitrary operating frequency of the interface. If exact timing is less critical it can be connected to the BITCLK signal.

4.3.2 CLKTTC: Clock for TTC-B-01 data (O)

This output is intended to be connected to the TTC-B-01 interface clock input of a Packet TC decoder. CLKTTC changes state on the falling CLCWCLK edge.

4.3.3 SAMPLE: Sample signal (O)

This output is intended to be connected to the TTC-B-01 interface sample input of a Packet TC decoder. SAMPLE changes state on the falling CLCWCLK edge.

4.3.4 D0TTC, D1TTC: Serial data (I)

These Schmitt trigger inputs retrieve CLCW data from the Packet TC decoder. They shall be stable on the falling CLKTTC edge.

4.3.5 SELCLCW: Select CLCW (I)

This CMOS input represents the value for bit 13 in the CLCW. It also selects which of the D0TTC and D1TTC inputs is used for the CLCW data. SELCLCW is latched on the falling SAMPLE edge.

4.3.6 TCID3, TCID4: Part of CLCW Virtual Channel identifier field (I)

These CMOS inputs represent the value for bits 11 and 12 in the CLCW and are latched on the falling SAMPLE edge.

4.3.7 RFAVAIL*: RF signal present (I)

This asynchronous Schmitt trigger input represents the value for bit 16 in the CLCW. It shall be asserted (= 0) when the RF signal is presented to the demodulators. The synchronizer incurs a delay of two BITCLK cycles.

4.3.8 BITLOCK*: Demodulator achieved bit lock (I)

This asynchronous Schmitt trigger input represents the value for bit 17 in the CLCW. It shall be asserted (= 0) when at least one of the demodulators has achieved bit lock. The synchronizer incurs a delay of two BITCLK cycles.

4.4 Transfer Frame output signals, 5 pins

4.4.1 SOUT: Serial Transfer Frame Output (O)

Serial bit stream data output. This is the complete Virtual Channel Frame plus Synchronization Marker, followed by the optional space for Reed-Solomon check codes. SOUT changes state on the falling BITCLK edge. One bit is output per BITCLK cycle.

4.4.2 ALTSOUT: Alternate Serial Transfer Frame Output (O)

This output is the same as SOUT except that it uses the Alternate Attached Synchronisation Marker. ALTSOUT changes state on the falling BITCLK edge.

4.4.3 SYNCMARK: Synchronisation Marker indication (O)

This output is asserted (= 1) when the Synchronisation Marker is output. This signal may be used to detect the Synchronisation Marker. SYNCMARK changes state on the falling BITCLK edge.

4.4.4 FRAME: Frame indication (O)

This output is asserted (= 1) when the Transfer Frame itself is output and is intended to be connected to the MA1916 SMC input. FRAME changes state on the falling BITCLK edge.

4.4.5 ODDFRAME: Odd Master Frame Counter indication (O)

This output has the same value as the least significant bit of the Master Channel Frame Counter. It changes state on the falling BITCLK edge, one BITCLK cycle before SYNCMARK is asserted.

4.5 Operational mode selection, 16 pins

These inputs define the operational mode of the VCM.

4.5.1 LEN0, LEN1: Transfer Frame Length selection (I)

These static CMOS inputs define the length of the Transfer Frame and the length of the space for the Reed-Solomon check codes:

LEN0	LEN1	Transfer Frame length	Length of space for check codes
0	0	223 octets	32 octets
0	1	446 octets	64 octets
1	0	892 octets	128 octets
1	1	1115 octets	160 octets

4.5.2 OPCF, FECW: Trailer insertion (I)

These static CMOS inputs define that the VCM shall insert a trailer according to:

OPCF	FECW	Resulting trailer
0	0	No trailer inserted
0	1	Frame Error Control Word
1	0	Operational Control Field
1	1	Operational Control Field and Frame Error Control Word

These inputs also affect the expected length of the PVCF received from the VCAs. The OPCF bit in the Transfer Frame Header is given the same value as the OPCF input.

4.5.3 RSSPACE: Insertion of space for Reed-Solomon check codes (I)

This static CMOS input defines whether the space for Reed-Solomon check codes is inserted (RSSPACE = 1) or not.

4.5.4 SCID0 to SCID9: Spacecraft identifier (I)

These static CMOS inputs define the 10-bit Spacecraft Identifier in the Transfer Frame Header.

4.5.5 EXTSEL: External Selection of next Virtual Channel (I)

This CMOS input selects one of three modes for the selection of the next Virtual Channel to output a Transfer Frame:

- When EXTSEL is static logic 0 Bandwidth Allocation is used.
- When EXTSEL is connected to the SYNCMARK output Priority Selection is used.
- When EXTSEL is static logic 1 the internal algorithms are not used. Instead the value present on the inputs RTS0 to RTS2 is used for the selection.

4.6 Miscellaneous, 11 pins

4.6.1 TEST0, TEST1: Test control (I)

These static CMOS inputs are used to set the VCM in test modes. TEST0 is used for controlling the internal BIST, which will be performed after reset when TEST0 = 0. TEST1 is used for production test and should always be tied to logic 0.

4.6.2 BITCLK: Clock (I)

This CMOS input is the bit clock.

4.6.3 RESET* (I)

This asynchronous Schmitt trigger input resets the VCM. The BIST is activated after the rising RESET* edge if the input TEST0 = 0. After the BIST is completed all registers are reset and the VCM starts with normal operation.

4.6.4 ERR*: Internal error detected (O)

This output indicates that an internal error has been detected. During reset and BIST ERR* is asserted (= 0). If no error was detected during the self-test ERR* is de-asserted. ERR* changes state on the falling BITCLK edge.

4.6.5 VCC, GND: Power and ground

Three pins of each.

5 ELECTRICAL AND MECHANICAL DATA

The VCM has been designed for the full military temperature range in the ABB Hafo SOS4 2 µ CMOS/SOS process. The die has an area of 63 mm^2 and contains 24k transistors. The VCM is a fully static design.

5.1 Absolute maximum ratings

Storage temperature	-65 °C to +150 °C
Operating ambient temperature	-55 °C to +125 °C
Supply voltage, V_{CC}	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{CC} + 0.5 V
DC input current (any pin)	±20 mA
Power dissipation	200 mWdc
Output dissipation	50 mWdc/output
ESD minimum critical path failure voltage	1500 V [1]
Total dose tolerance	> 100 kRad (Si)
Latch-up	Immune

1) Categorized as Class 2.

5.2 DC specifications

Valid over the full functional operating range; V_{CC} = 5 V ± 10%, T_{CASE} = -55 °C to +125 °C, after 100 kRad irradiation.

Parameter	Min	Max	Condition
CMOS inputs:			
Input low voltage	0.0 V	1.3 V	
Input high voltage	3.9 V	V_{CC}	
Input leakage current		±5 µA	BITCLK input, $0 \le V_{IN} \le V_{CC}$
Input leakage current		±1 µA	Other inputs, $0 \le V_{IN} \le V_{CC}$
Capacitance [1]		5 pF	
TTL inputs:			
Input low voltage	0.0 V	0.8 V	
Input high voltage	2.0 V	V_{CC}	
Input leakage current		±1 µA	$0 \le V_{IN} \le V_{CC}$
Capacitance [1]		5 pF	

Parameter	Min	Max	Condition
Schmitt trigger inputs:			
Input low trigger voltage		1.0 V	
Input high trigger voltage	V_{CC}-1.2 V		
Schmitt trigger hysteresis	0.5 V		
Input leakage current		±1 µA	$0 \le V_{IN} \le V_{CC}$
Capacitance [1]		5 pF	
Outputs: [2]			
Output low voltage		0.40 V	I = 4 mA
Output high voltage	V_{CC}-0.6 V		I = 4 mA
Output leakage current		20 µA	Tristate, $0 \le V_{OUT} \le V_{CC}$
Capacitance [1]		10 pF	
TTL Bidirectional signals:			
Input low voltage	0.0 V	0.8 V	
Input high voltage	2.0 V	V_{CC}	
Output low voltage		0.40 V	I = 4 mA
Output high voltage	V_{CC}-0.6 V		I = 4 mA
Output leakage current		20 µA	Tristate, $0 \le V_{OUT} \le V_{CC}$
Capacitance [1]		10 pF	
Power dissipation: [3]			
Static dissipation [4]		20 mW	
Dynamic dissipation		10 mW/MHz	Normal operation
Dynamic dissipation		35 mW/MHz	During BIST
TTL input [5]		0.05 mW/input	V_{IN} = 0.8 V
TTL input [5]		3.5 mW/input	V_{IN} = 2.4 V

1) Capacitance values include the pad and the pin.

2) The outputs are compatible with both CMOS and TTL level inputs.

3) With 25 pF load on all outputs. The total power dissipation is the sum of the static dissipation, the dynamic dissipation at the operational frequency and the TTL input dissipation.

4) The high value for the static dissipation is due to the leakage current at high temperatures.

5) The TTL dissipation depends on the input voltage and is close to zero when the input is held at 0 V or V_{CC}. TTL level inputs should therefore be driven as close as possible to the end voltages.

5.3 AC specifications

All timing values are valid for the full operational temperature range, radiation range and power supply range, with 25 pF output load (add 8 ns to the output delays for 50 pF load).

No.	Description	Min	Max
T_{RES}	RESET* asserted	3 T_{BCK}	
f_{BCK}	BITCLK frequency	0 Hz	12.5 MHz
T_{BCK}	BITCLK period	80 ns	
T_{BLO}	BITCLK low	40 ns	
T_{BHI}	BITCLK high	40 ns	
T_{CCK}	CLCWCLK period	80 ns	
T_{CLO}	CLCWCLK low	40 ns	
T_{CHI}	CLCWCLK high	40 ns	
T_1	RTS, PVCF setup time to BITCLK low	5 ns	
T_2	RTS, PVCF hold time after BITCLK low	10 ns	
T_3	RTS setup time to SYNCMARK high (ext. selection)	2 T_{BCK}	
T_4	RTS hold time after SYNCMARK high (ext. selection)	2 T_{BCK}	
T_5	BITCLK low to POLL, CTS, SOUT, FRAME, ODDFRAME stable		32 ns
T_6	BITCLK low to ALTSOUT, SYNCMARK stable		35 ns
T_7	D0TTC, D1TTC setup time to CLKTTC low	60 ns	
T_8	D0TTC, D1TTC hold time after CLKTTC low	0 ns	
T_9	SELCLCW, TCID setup time to SAMPLE low [1]	2 T_{CCK}	
T_{10}	SELCLCW, TCID hold time after SAMPLE low [1]	2 T_{CCK}	
T_{11}	R/W* low to CS* low	0 ns	
T_{12}	CS* high to R/W* high	5 ns	
T_{13}	CS* width asserted	50 ns	
T_{14}	CS* width de-asserted after write	4 T_{BCK}	
T_{15}	Write A, D setup time to CS* high	10 ns	
T_{16}	Write A, D hold time after CS* high	10 ns	
T_{17}	CS* low to D valid		45 ns
T_{18}	Read A valid to D valid		60 ns
T_{19}	CS* high to D tristate		35 ns

[1)] Violation will only lead to uncertainty about which values were latched.

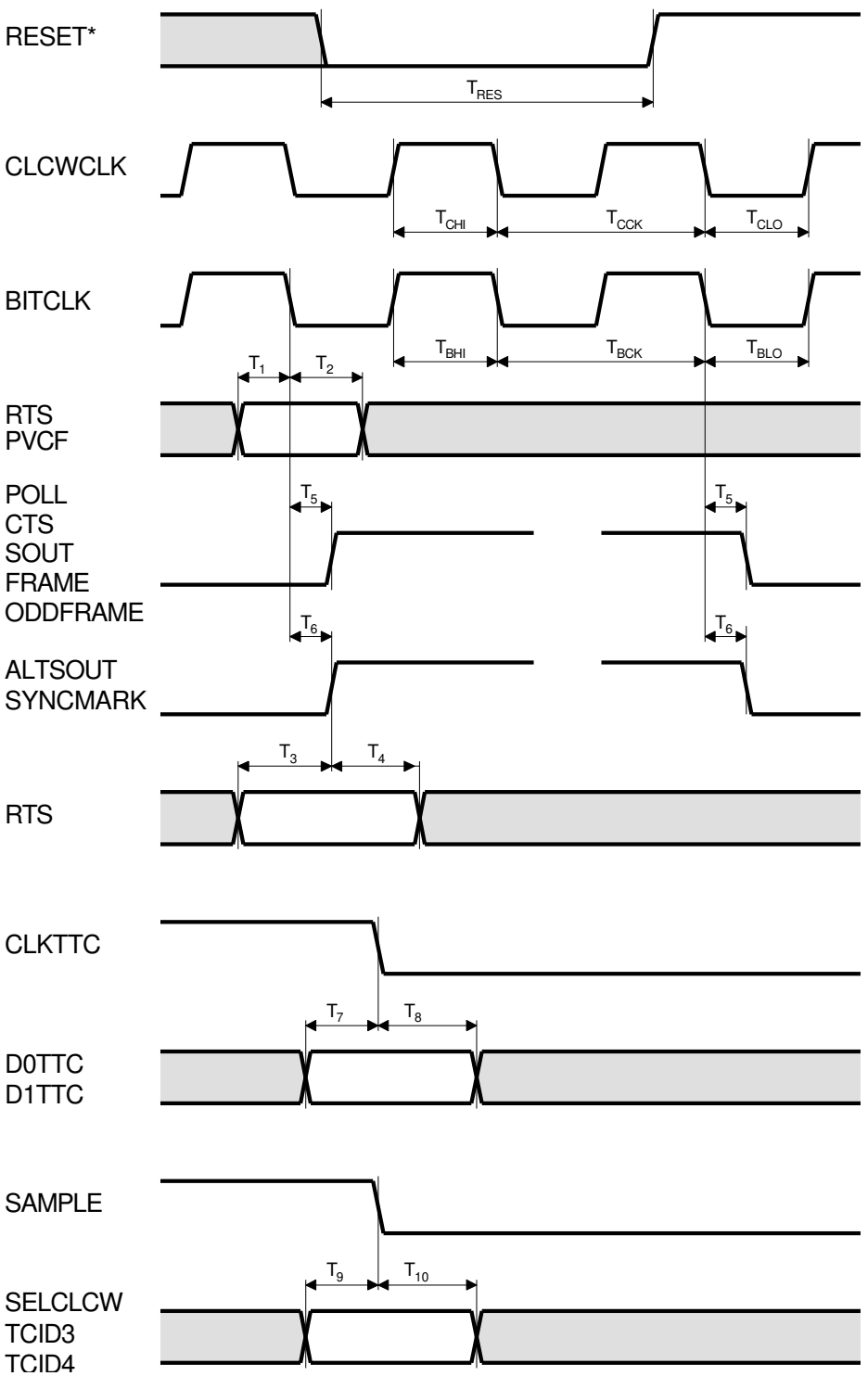

Figure 6: Timing of various signals

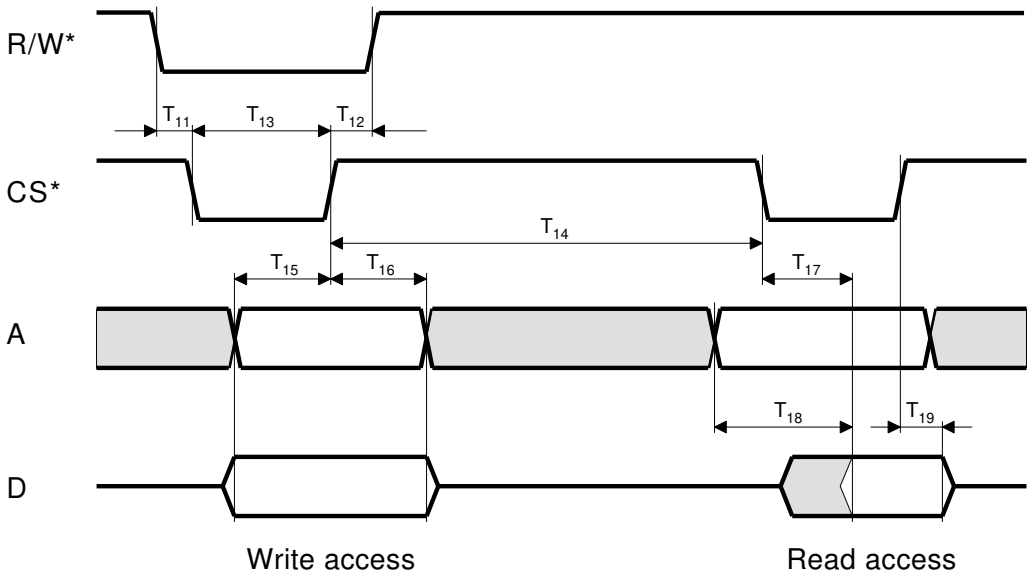

Figure 7: Timing of various signals (continued)

5.4 Mechanical data

5.4.1 Pin assignment

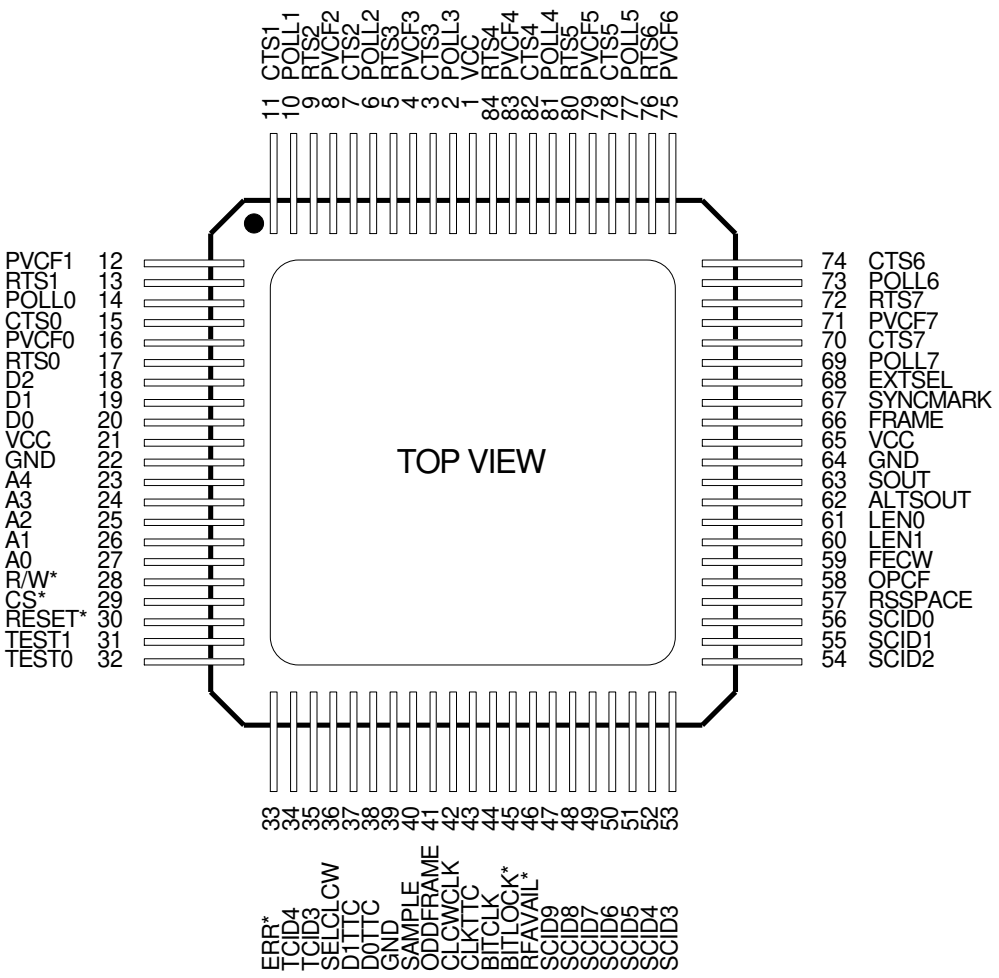

Figure 8: VCM pin assignment

5.4.2 Package dimensions

The VCM is available in an 84 pin Ceramic Quad Flat Package with 25-mil pin pitch.

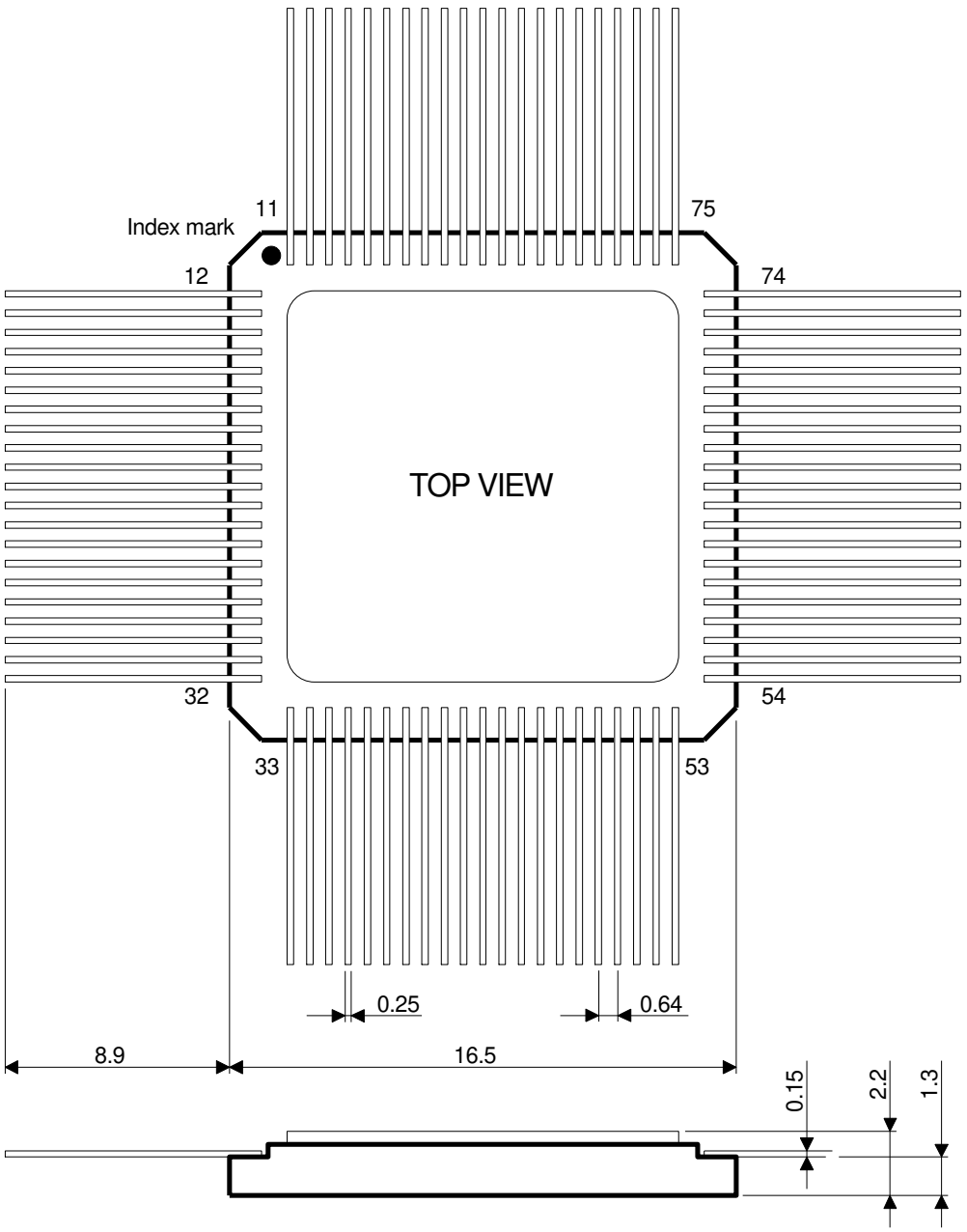

Figure 9: Dimensions for 25 mil pin pitch Ceramic Quad Flat Pack (mm)

6 ABBREVIATIONS

BAT	Bandwidth Allocation Table
BIST	Built-In Self Test
CCSDS	Consultative Committee for Space Data Systems
CLCW	Command Link Control Word
CTS	Clear To Send
ESA	European Space Agency
ESD	Electrostatic Discharge
FECW	Frame Error Control Word
ID	Identification
LSB	Least Significant Bit
OPCF	Operational Control Field
PVCF	Partial Virtual Channel Frame
RS	Reed-Solomon
RTS	Ready To Send
SEU	Single Event Upset
SOS	Silicon On Sapphire
TC	Telecommand
TTC-B-01	Obsolete standard
VC	Virtual Channel
VCM	Virtual Channel Multiplexer
VCA	Virtual Channel Assembler

Appendix A: Selection algorithm examples

Example of next Virtual Channel to output a Transfer Frame selection

For the examples below, the entries in the BAT are:

0, 1, 0, 2, 0, 3, 0, 1, 0, 2, 0, 3, 0 ... etc.

The following number of complete PVCFs will become available from the VCAs:

VC0: three PVCFs
VC1: one PVCF
VC2: none
VC3: two PVCFs
VC4: two PVCFs
VC7: none

The examples below show what would be output directly after reset, with the BAT programmed as described above before the selection starts. The value of the BAT pointer is initially 0, i.e. pointing to the first entry in the list above.

Using the Bandwidth Allocation algorithm, the Transfer Frames output from the VCM will be from:

(First after reset) **VC7(Idle) VC0 VC1 VC0** (VC2 no frame) **VC0 VC3** (VC0, VC1, VC0, VC2, VC0 no frame) **VC3** (none of the entries in the BAT has a frame) **VC7(Idle) VC7(Idle)** ...

Similarly, by employing the Priority Selection algorithm, the Transfer Frames output from the VCM will be from:

VC7(Idle) VC0 VC0 VC0 VC1 VC3 VC3 VC7(Idle) VC7(Idle) ...

Finally, using External Selection with RTS0 = RTS1 = RTS2 = 0 as e.g. in a simple system using only one VCA, the following Transfer Frames will be output (the first Transfer Frame is idle since no data have been gathered after reset):

VC0(Idle) VC0 VC0 VC0 VC0(Idle) VC0(Idle) ...

Note that no Transfer Frames are generated for Virtual Channel 4 since there is no entry in the BAT indicating VC4.

Adaptive frame ordering versus fixed frame ordering

Fixed frame ordering has the following characteristics:

- The sequence of Virtual Channels to output a Transfer Frame is fixed, though this sequence may be changed for different phases of a mission.

- If a Virtual Channel selected for output has not enough data to output a Transfer Frame, it instead generates an idle frame which can be regarded as originating from the Virtual Channel, but without any valid data. The Virtual Channel Count is updated.

This means that some of the bandwidth may not be utilized, if the data source(s) associated with a Virtual Channel continuously do not produce exactly the amount of data that it has bandwidth allocated for. Therefore, the VCM built-in algorithms use adaptive frame ordering that dynamically may alter the frame ordering:

- As long as all Virtual Channels in the sequence can output a Transfer Frame, the sequence is followed.

- If the Virtual Channel selected for output is not able to output a Transfer Frame, that Virtual Channel is considered as being in the OFF state and the next Virtual Channel in the sequence is selected for output. Thus, in the normal case, the Transfer Frame Generator does not produce idle frames and the bandwidth can be used for Transfer Frames from other Virtual Channels.

- In the case that none of the Virtual Channels can output a Transfer Frame, the VCM has to output an idle frame, which thus is not associated with any particular Virtual Channel. However, in order to be compliant with RD1, the VCM built-in selection algorithms use VCA 7 for producing an idle PVCF.

Appendix B: Asynchronous CLCW input interface

Although normally intended to be connected to the same clock as BITCLK, CLCWCLK may be connected to a different asynchronous clock, allowing a transfer rate independent of the bit rate.

If CLCWCLK has a lower frequency than BITCLK, the acquisition may span several Transfer Frames. The number of Transfer Frames output for each acquisition can be calculated as the nearest integer higher than

$$\frac{160 \bullet f_{BCK}}{(4 + (\text{frame length}) + (\text{RS length})) \bullet f_{CCK}}$$

For example, if f_{BCK} = 10 MHz, f_{CCK} = 1 MHz, and 223 octet Transfer Frames with Reed-Solomon encoding are used, $(160 \bullet 10/((4 + 223 + 32) \bullet 1) = 6.18 \Rightarrow 7$ Transfer Frames will be output for each acquired CLCW. Combinations that give a ratio close to the integer limit (e.g. 1.99 or 2.0) should be avoided; it can give a varying number of Transfer Frames per CLCW acquisition (or in very rare cases without FECW and Reed-Solomon check codes, leading to the OPCF not being updated due to a design shortcoming).

In the case that the CLCW acquisition spans several Transfer Frames, the VCA will output the previously retrieved CLCW value until a new acquisition is completed. The first Transfer Frame after reset would then have bits 18 - 31 equal to 0. In case SAMPLE is rising while the CLCW is being output, the update is delayed until the old CLCW has been output.

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ABB HAFO AB
P.O. Box 520 S-175 26 JÄRFÄLLA SWEDEN Telephone +46 (0)8 580 24500 Telex 172 62 Telefax +46 (0)8 580 31952