Accelerator Series FPGAs – ACT™ 3 Family

Features

- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)
- Highly Predictable Performance with 100% Automatic Placement and Routing
- 7.5 ns Clock-to-Output Times
- Up to 250 MHz On-Chip Performance
- Up to 228 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More than 500 Macro Functions
- Replaces up to twenty 32 macro-cell CPLDs
- Replaces up to one hundred 20-pin PAL® Packages
- Up to 1153 Dedicated Flip-Flops
- VQFP, TQFP, BGA, and PQFP Packages
- Nonvolatile, User Programmable
- Fully Tested Prior to Shipment
- 5.0V and 3.3V Versions
- Optimized for Logic Synthesis Methodologies
- Low-power CMOS Technology

Device	A1415	A1425	A1440	A1460	A14100
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Packages (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules	200	310	564	848	1,377
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops[1]	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Packages[2] (by pin count)					
CPGA	100	133	175	207	257
PLCC	84	84	84	—	—
PQFP	100	100, 160	160	160, 208	—
RQFP	—	—	—	—	208
VQFP	100	100	100	—	—
TQFP	—	—	176	176	—
BGA	—	—	—	225	313
CQFP	—	132	—	196	256
Performance[3] (maximum, worst-case commercial)					
Chip-to-Chip[4]	108 MHz	108 MHz	100 MHz	97 MHz	93 MHz
Accumulators (16-bit)	63 MHz	63 MHz	63 MHz	63 MHz	63 MHz
Loadable Counter (16-bit)	110 MHz	110 MHz	110 MHz	110 MHz	105 MHz
Prescaled Loadable Counters (16-bit)	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Datapath, Shift Registers	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Clock-to-Output (pad-to-pad)	7.5 ns	7.5 ns	8.5 ns	9.0 ns	9.5 ns

Notes:

1. *One flip-flop per S-Module, two flip-flops per I/O-Module.*
2. *See product plan on page 1-178 for package availability.*
3. *Based on A1415A-3, A1425A-3, A1440B-3, A1460B-3, and A14100B-3.*
4. *Clock-to-Output + Setup*

Description

Actel's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high perfomance, PCI compliant programmable solution capable of 250 MHz on-chip performance and 7.5 nanosecond clock-to-output, with capacities spanning from 1,500 to 10,000 gate array equivalent gates. For further information regarding PCI compliance of ACT 3 devices, see "Accelerator Series FPGAs—ACT 3 PCI Compliant Family."

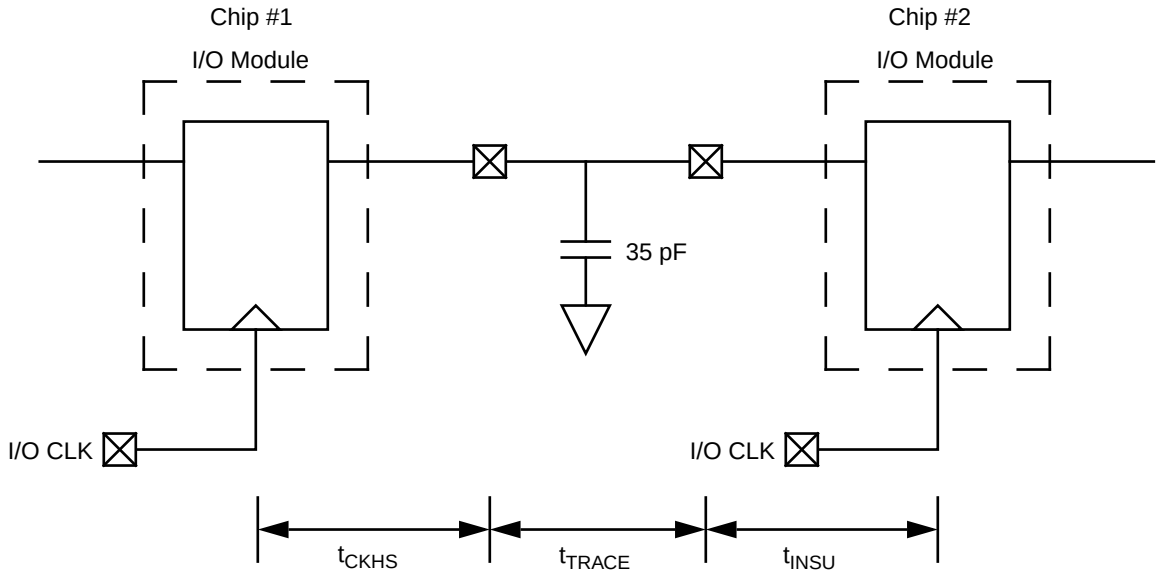
The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Actel's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 7.5 nanosecond clock-to-out times. The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output enables.

The ACT 3 family is supported by Actel's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing anlaysis, user programming, and debug and diagnostic probe capabilities. The Designer Series is supported on the following platforms: 486/Pentium class PC's, Sun®, and HP®, workstations. The software provides CAE interfaces to Cadence, Mentor Graphics®, OrCAD™ and Viewlogic®, design environments. Additional platforms are supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

Predictable Performance* (Worst-Case Commercial)

Accumulators (16-bit)	63 MHz
Loadable Counters (16-bit)	110 MHz
Prescaled Loadable Counters (16-bit)	250 MHz
Shift Registers	250 MHz

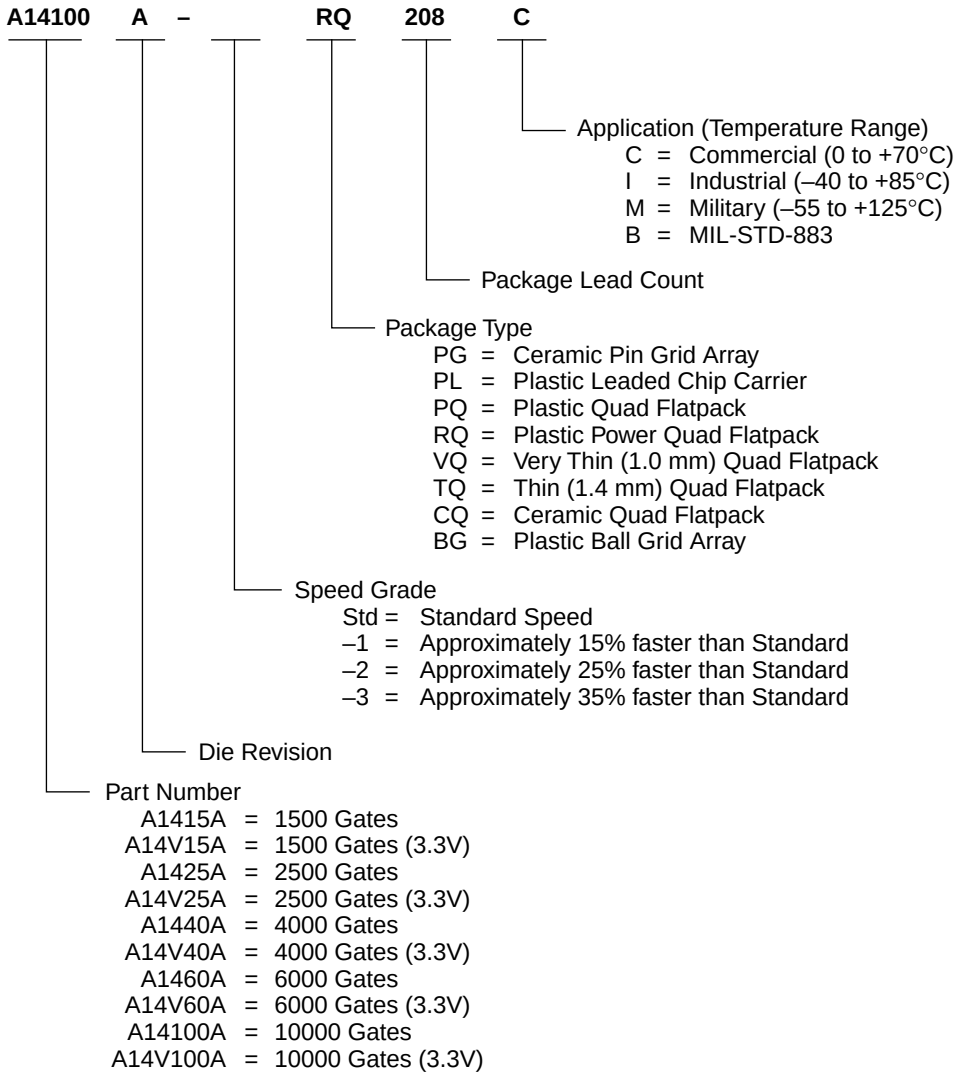
System Performance Model



Chip-to-Chip Performance (Worst-Case Commercial)

	t_{CKHS}	t_{TRACE}	t_{INSU}	Total	MHz
A1425A-3	7.5	1.0	1.8	10.3 ns	97
A1460A-3	9.0	1.0	1.3	11.3 ns	88

Ordering Information



Product Plan

	Speed Grade*				Application			
	Std	–1	–2	–3	C	I	M	B
A1415A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	✔	—	—
100-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—	—	—
A14V15A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	—	—	—	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	—	—	—	✔	—	—	—
A1425A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	✔	—	—
132-pin Ceramic Quad Flatpack (CQFP)	✔	✔	—	—	✔	—	✔	✔
133-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔†	✔†	✔	—	✔	✔
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
A14V25A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	—	—	—	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	—	—	—	✔	—	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	—	—	—	✔	—	—	—
A1440A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	—	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
175-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	✔	✔	✔	✔	—	—	—
A14V40A Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	—	—	—	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	—	—	—	✔	—	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	—	—	—	✔	—	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	—	—	—	✔	—	—	—
A1460A Device								
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	P	✔	✔	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	✔	✔	P	✔	✔	—	—
196-pin Ceramic Quad Flatpack (CQFP)	✔	✔	—	—	✔	—	✔	✔
207-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔†	P†	✔	—	✔	✔
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	P	✔	✔	—	—
225-pin Platic Ball Grid Array (BGA)	✔	✔	✔	P	✔	—	—	—

Applications: *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883* † *Commercial Only*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

** Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35 % faster than Standard.*

Product Plan (continued)

	Speed Grade*				Application			
	Std	–1	–2	–3	C	I	M	B
A14V60A Device								
160-pin Plastic Quad Flatpack (PQFP)	✔	—	—	—	✔	—	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	—	—	—	✔	—	—	—
208-pin Plastic Quad Flatpack (PQFP)	✔	—	—	—	✔	—	—	—
A14100A Device								
208-pin Power Quad Flatpack (RQFP)	✔	✔	✔	✔	✔	✔	—	—
257-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔†	✔†	✔	—	✔	✔
313-pin Plastic Ball Grid Array (BGA)	✔	✔	✔	✔	✔	—	—	—
256-pin Ceramic Quad Flatpack (CQFP)	✔	✔	—	—	✔	—	✔	✔
A14V100A Device								
208-pin Power Quad Flatpack (RQFP)	✔	—	—	—	✔	—	—	—
313-pin Plastic Ball Grid Array (BGA)	✔	—	—	—	✔	—	—	—

Applications: *C = Commercial*, *I = Industrial*, *M = Military*, *B = MIL-STD-883*, † *Commercial Only*

Availability: ✔ = *Available*, *P = Planned*, — = *Not Planned*

** Speed Grade:* *–1 = Approx. 15% faster than Standard*, *–2 = Approx. 25% faster than Standard*, *–3 = Approx. 35 % faster than Standard.*

Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PLCC	PQFP, RQFP			VQFP	TQFP	BGA	
			84-pin	100-pin	160-pin	208-pin	100-pin	176-pin	225-pin	313-pin
A1415	200	1500	70	80	—	—	80	—	—	—
A1425	310	2500	70	80	100	—	83	—	—	—
A1440	564	4000	70	—	131	—	83	140	—	—
A1460	848	6000	—	—	131	167	—	151	168	—
A14100	1377	10000	—	—	—	175	—	—	—	228

Hermetic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			CPGA					CQFP		
			100-pin	133-pin	175-pin	207-pin	257-pin	132-pin	196-pin	256-pin
A1415	200	1500	80	—	—	—	—	—	—	—
A1425	310	2500	—	100	—	—	—	100	—	—
A1440	564	4000	—	—	140	—	—	—	—	—
A1460	848	6000	—	—	—	168	—	—	168	—
A14100	1377	10000	—	—	—	—	228	—	—	228

Pin Description

CLKA Clock A (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

DCLK Diagnostic Clock (Input)

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5 V Supply Voltage

HIGH supply voltage.

Architecture

This section of the data sheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 1.

Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules. The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module. S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11

where: S0 = A0 * B0 and S1 = A1 + B1

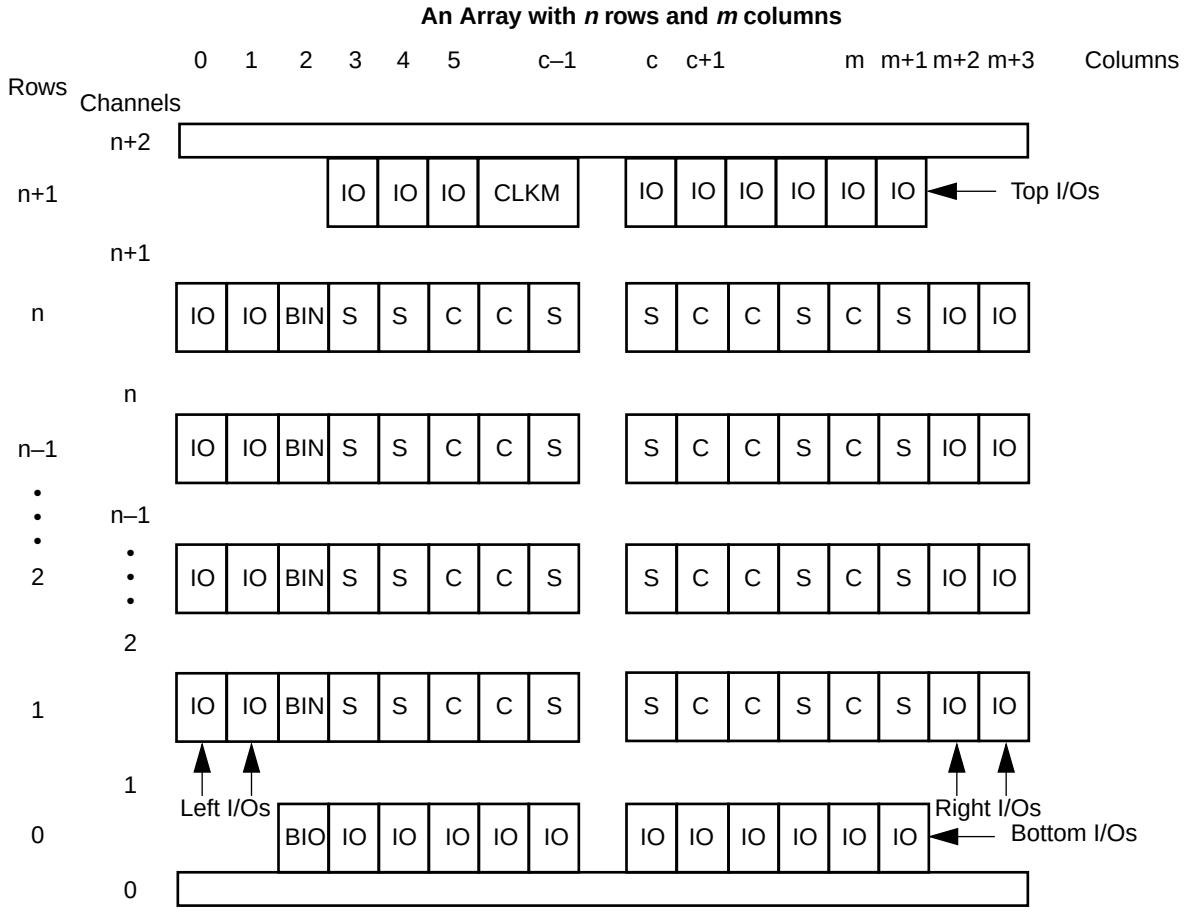


Figure 1 • *Generalized Floor Plan of ACT 3 Device*

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in Figures 2 and 3. The clock selection is determined by a multiplexor select at the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in Figure 4. The signals DataIn and DataOut connect to the I/O pad driver. Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

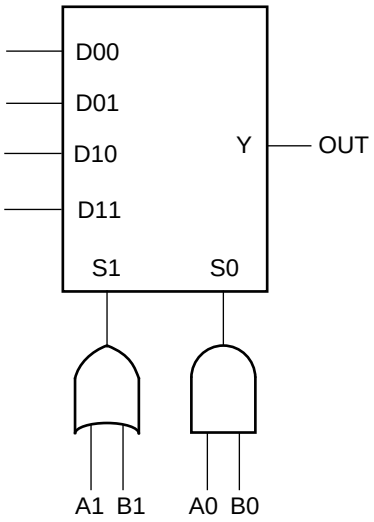


Figure 2 • *C-Module Diagram*

The I/O module output Y is used to bring Pad signals into the array *or* to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

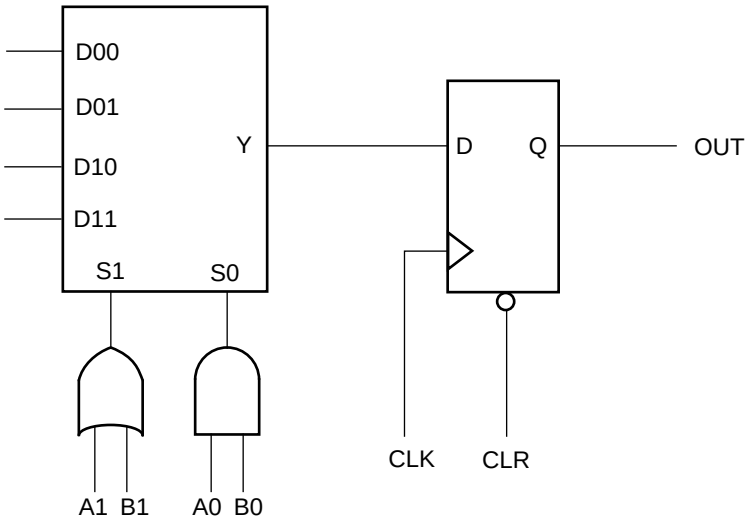


Figure 3 • *S-Module Diagram*

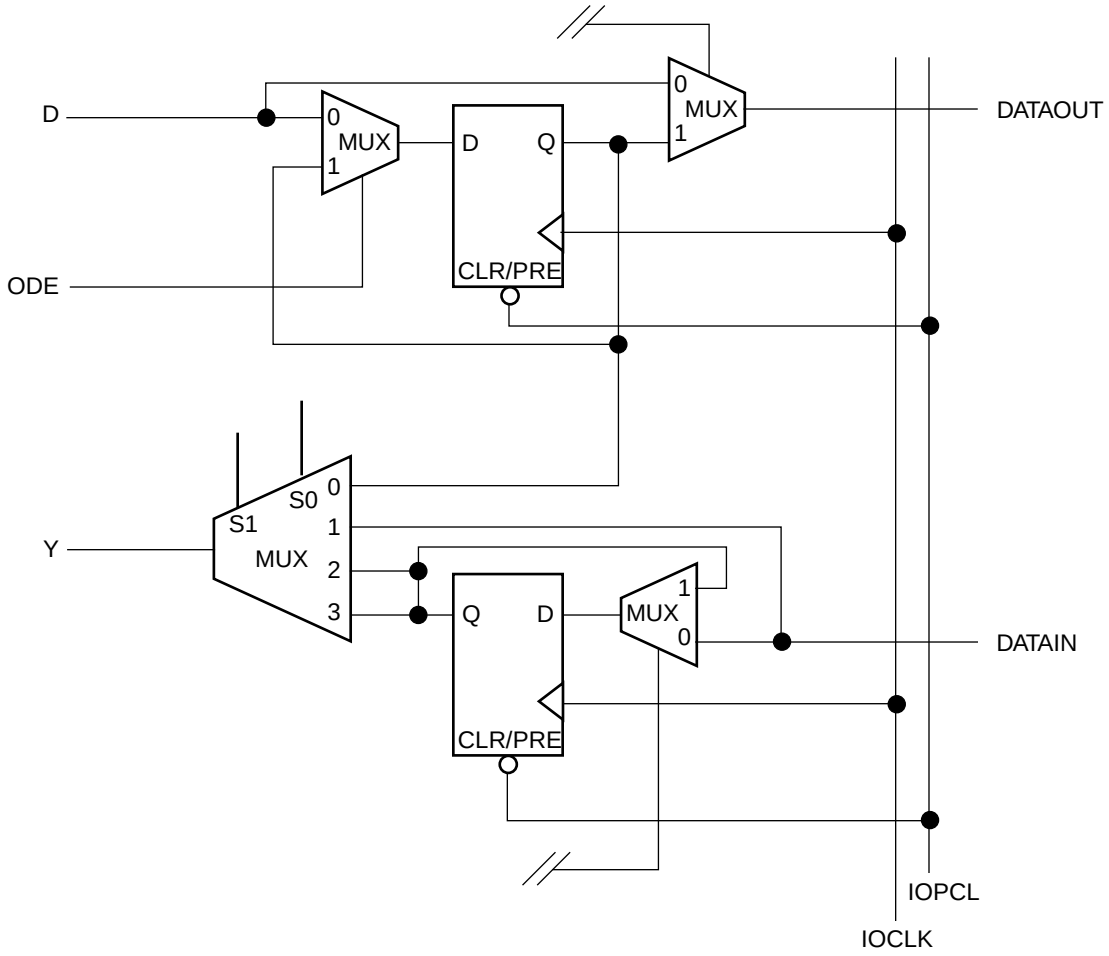


Figure 4 • *Functional Diagram for I/O Module*

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 5.

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

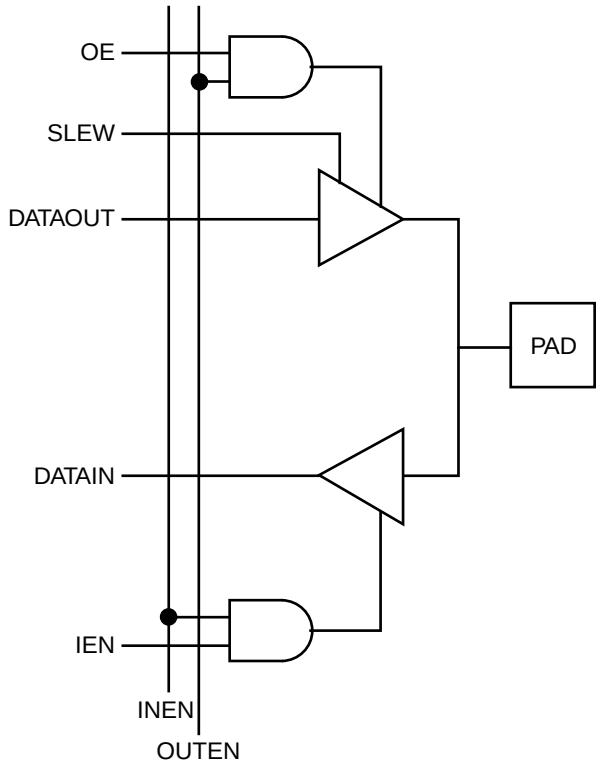


Figure 5 • *Function Diagram for I/O Pad Driver*

Routed Clocks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (see Figure 6):

- externally from the CLKA pad
- externally from the CLKB pad
- internally from the CLKINA input
- internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

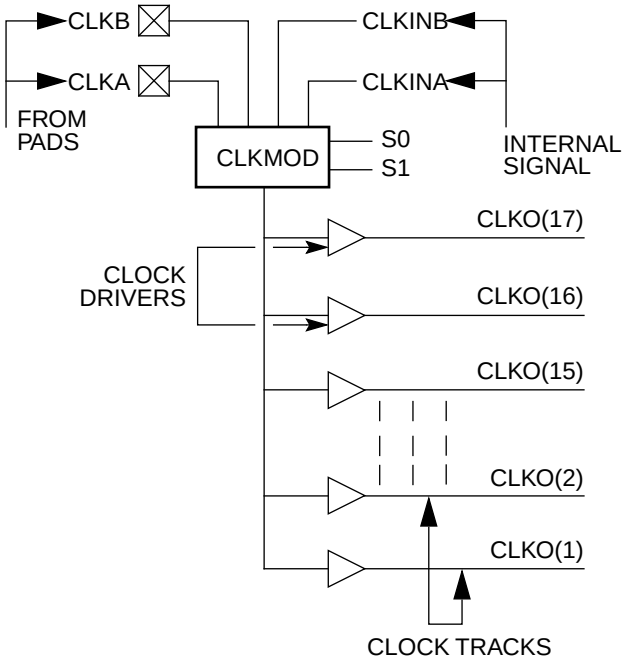


Figure 6 • *Clock Networks*

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during

routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

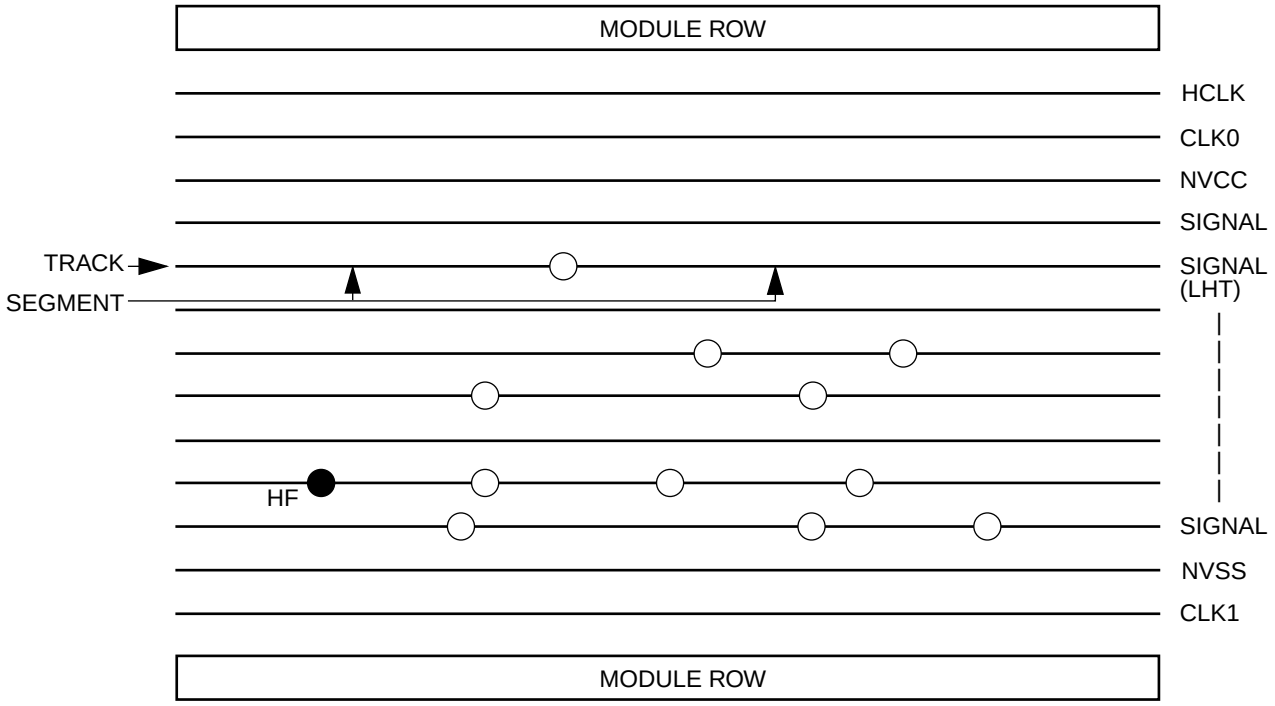


Figure 7 • *Horizontal Routing Tracks and Segments*

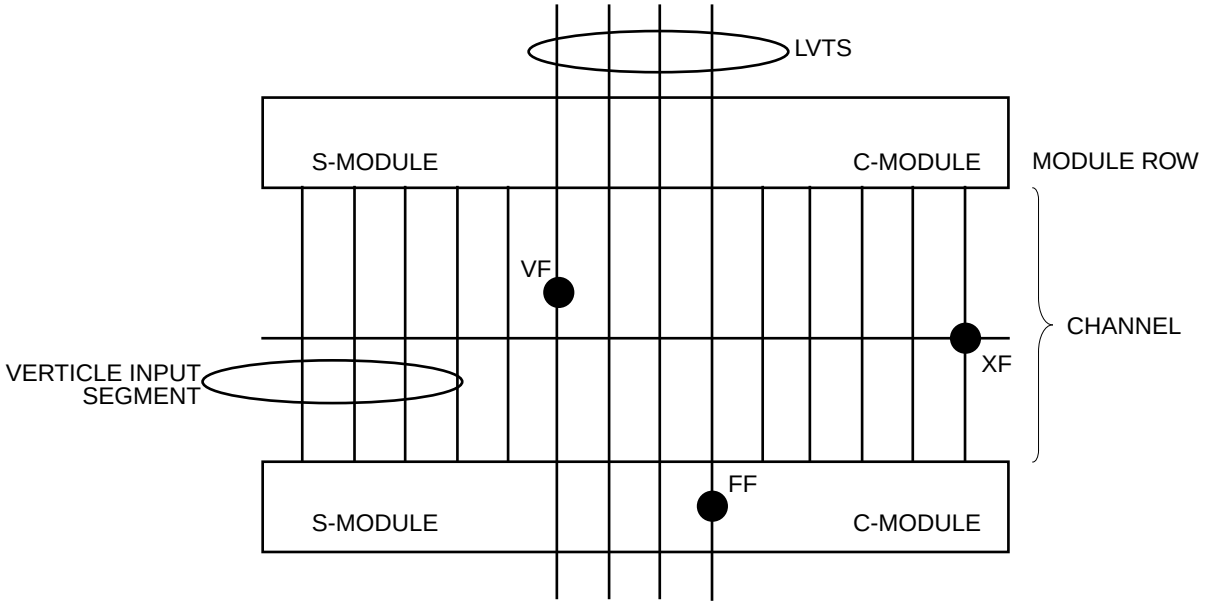


Figure 8 • *Vertical Routing Tracks and Segments*

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.) Table 1 shows four types of antifuses.

Table 1 • *Antifuse Types*

XF	Horizontal-to-Vertical Connection
HF	Horizontal-to-Horizontal Connection
VF	Vertical-to-Vertical Connection
FF	"Fast" Vertical Connection

Examples of all four types of connections are shown in Figures 7 and 8.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below as shown in Figure 9.

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

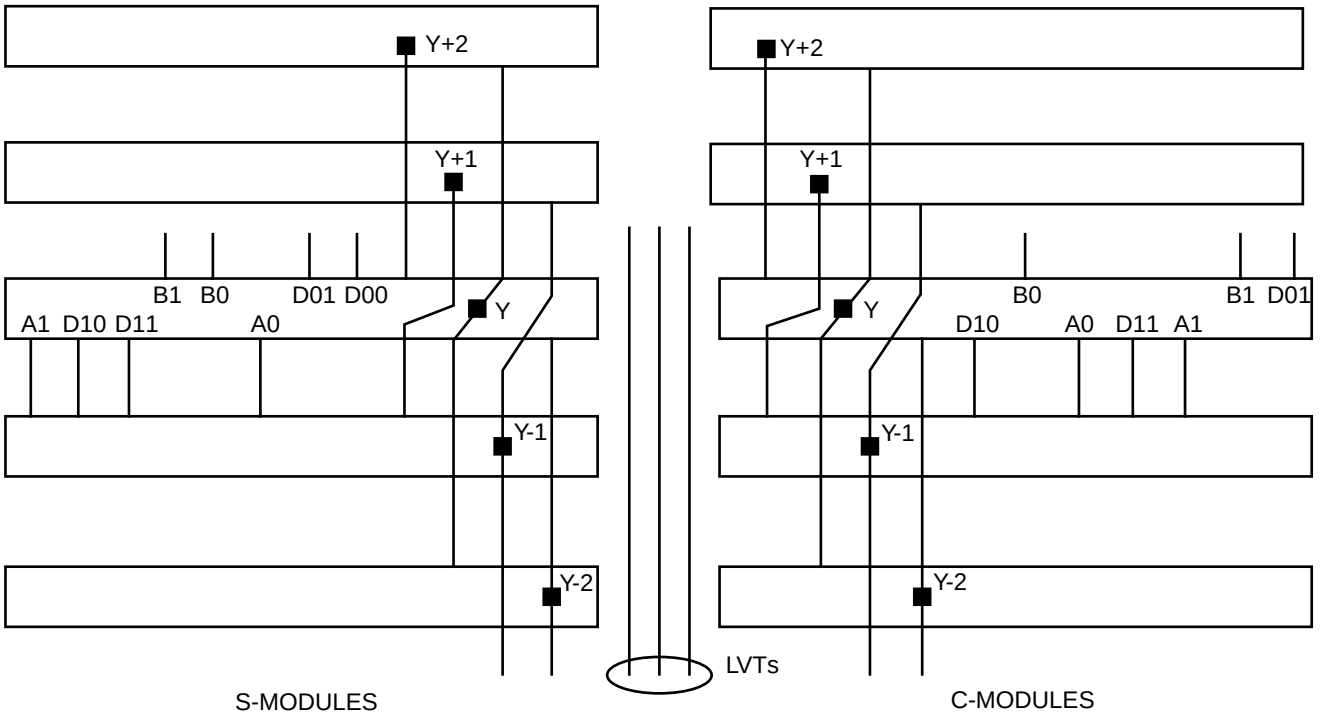


Figure 9 • *Logic Module Routing Interface*

5V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
5V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Industrial		Military		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1,2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)			3.7		3.7		V
		I_{OH} = –6 mA (CMOS)	3.84						V
		I_{OH} = –10 mA (TTL)[3]	2.40						V
V_{OL}[1,2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4		0.4	V
		I_{OL} = +12 mA (TTL)[3]		0.50					V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	V_I = V_{CC} or GND	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	3-state Output Leakage	V_O = V_{CC} or GND	–10	+10	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3,4]			10		10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current	(typical = 0.7 mA)		2		10		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See "Power Dissipation" Section							

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested, for information only.*
4. *V_{OUT} = 0V, f = 1 MHz.*
5. *Typical standby current = 0.7 mA. All outputs unloaded. All inputs = V_{CC} or GND.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	3.0 to 3.6	V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Units
		Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		V
	(I_{OH} = –3.2 mA)	2.4		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4	V
V_{IL}		–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4] (typical = 0.3 mA)			0.75	mA
Leakage Current[5]		–10	10	µA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.*
5. *V_O, V_{IN} = V_{CC} or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{25°C/W} = 3.2\ W$$

Package Type[1]	Pin Count	θjc	θja Still Air	θja 300 ft/min	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note:

1. *Maximum Power Dissipation in Still Air for 160-pin PQFP package is 2.4 Watts, 208-pin PQFP package is 2.4 Watts, 100-pin PQFP package is 1.6 Watts, 100-pin VQFP package is 1.9 Watts, 176-pin TQFP package is 2.5 Watts, 84-pin PLCC package is 2.2 Watts, 208-pin RQFP package is 4.7 Watts, 225-pin BGA package is 3.2 Watts, 313-pin BGA package is 3.5 Watts.*

Power Dissipation

$$P = [I_{CC\ standby} + I_{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M \quad (1)$$

Where:

$I_{CC\ standby}$ is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

I_{CC}	V_{CC}	Power
2mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 2.

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \quad (2)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	6.7
Input Buffers ($_{CEQI}$)	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads (C_{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 3 shows a piece-wise linear summation over all components.

$$\begin{aligned}\text{Power} = {} & V_{CC}2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} \\ & + (p * (C_{EQO} + C_L) * f_p)_{outputs} \\ & + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} \\ & + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} \\ & + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * CEQCD * f_{s1})_{dedicated\_Clk} \\ & + (s_2 * CEQCI * f_{s2})_{IO\_Clk}] \end{aligned} \quad (3)$$

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock

s_2 = Fixed number of clock loads on the dedicated I/O clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

fp = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

f_{s1} = Average dedicated array clock rate in MHz

f_{s2} = Average dedicated I/O clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1415A	60	60
A14V15A	57	57
A1425A	75	75
A14V25A	72	72
A1440A	105	105
A14V40A	100	100
A1440B	105	105
A1460A	165	165
A14V60A	157	157
A1460B	165	165
A14100A	195	195
A14V100A	185	185
A14100B	195	195

Fixed Clock Loads (s_1/s_2)

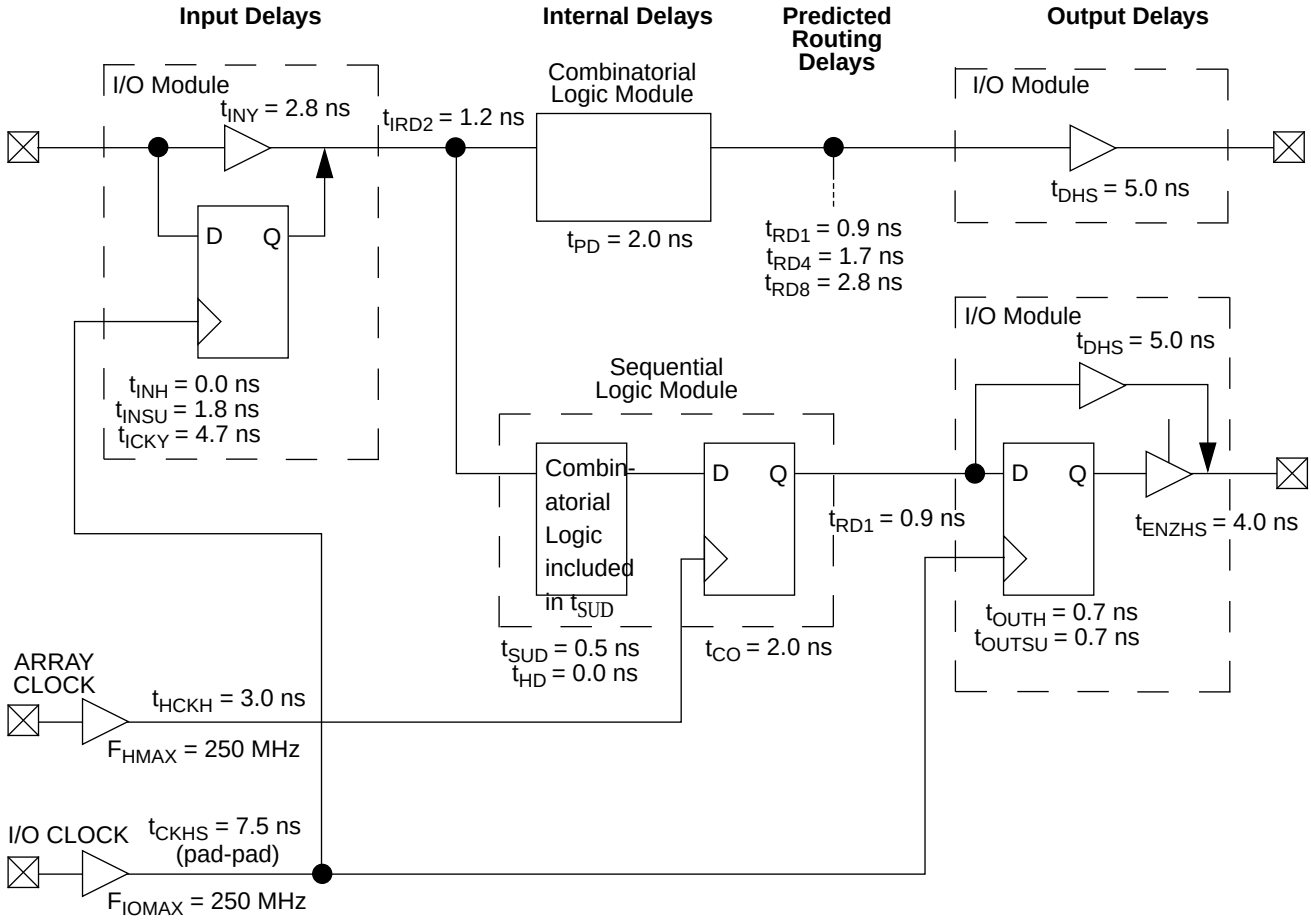
Device Type	s_1 Clock Loads on dedicated array clock	s_2 Clock Loads on dedicated I/O clock
A1415A	104	80
A14V15A	104	80
A1425A	160	100
A14V25A	160	100
A1440A	288	140
A14V40A	288	140
A1440B	288	140
A1460A	432	168
A14V60A	432	168
A1460B	432	168
A14100A	697	228
A14V100A	697	228
A14100B	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

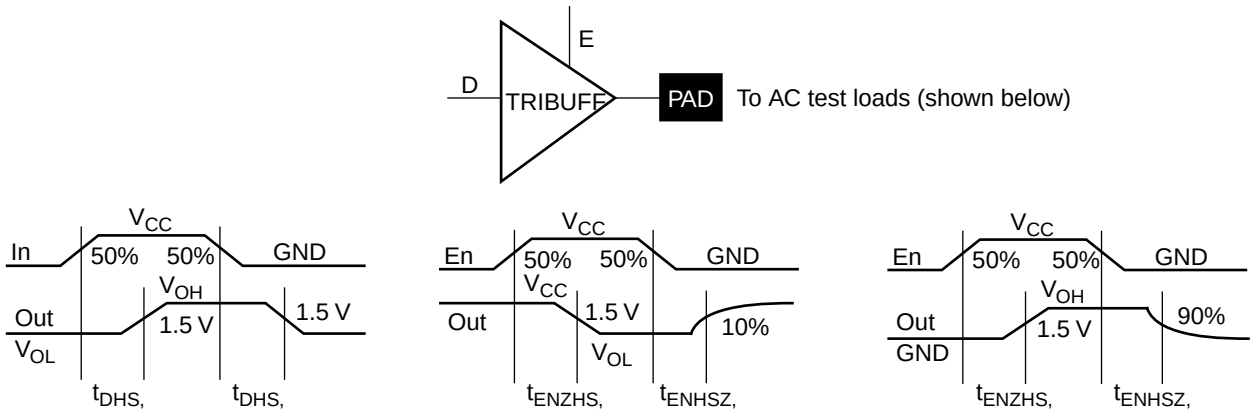
Logic Modules (m)	=	80% of modules
Inputs switching (n)	=	# inputs/4
Outputs switching (p)	=	# output/4
First routed array clock loads (q_1)	=	40% of sequential modules
Second routed array clock loads (q_2)	=	40% of sequential modules
Load capacitance (C_L)	=	35 pF
Average logic module switching rate (f_m)	=	F/10
Average input switching rate (f_n)	=	F/5
Average output switching rate (f_p)	=	F/10
Average first routed array clock rate (f_{q1})	=	F/2
Average second routed array clock rate (f_{q2})	=	F/2
Average dedicated array clock rate (f_{s1})	=	F
Average dedicated I/O clock rate (f_{s2})	=	F

ACT 3 Timing Model*



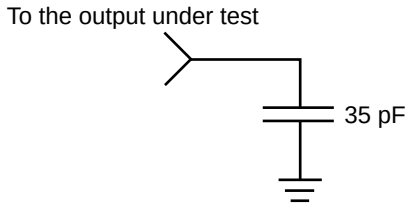
**Values shown for A1425A-3.*

Output Buffer Delays

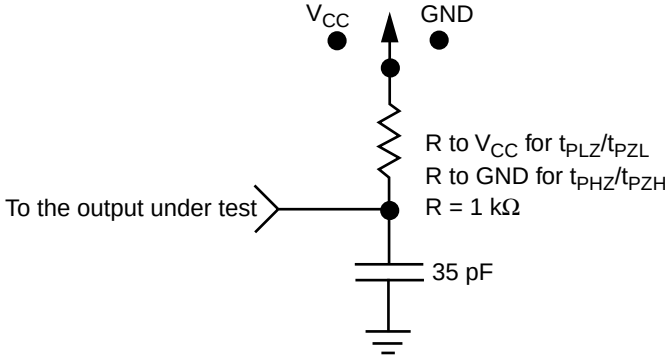


AC Test Loads

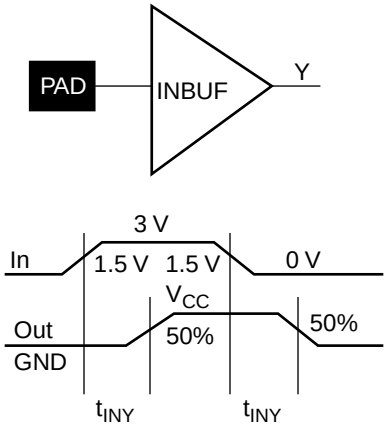
Load 1
(Used to measure propagation delay)



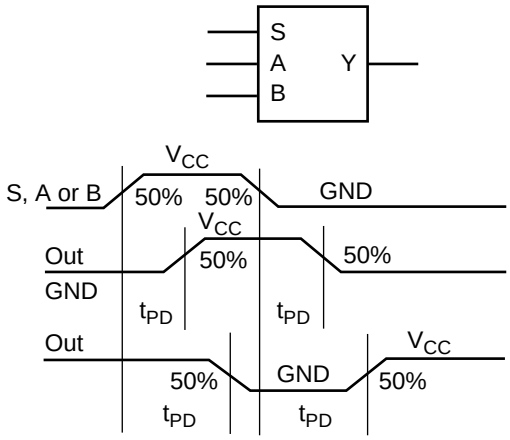
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

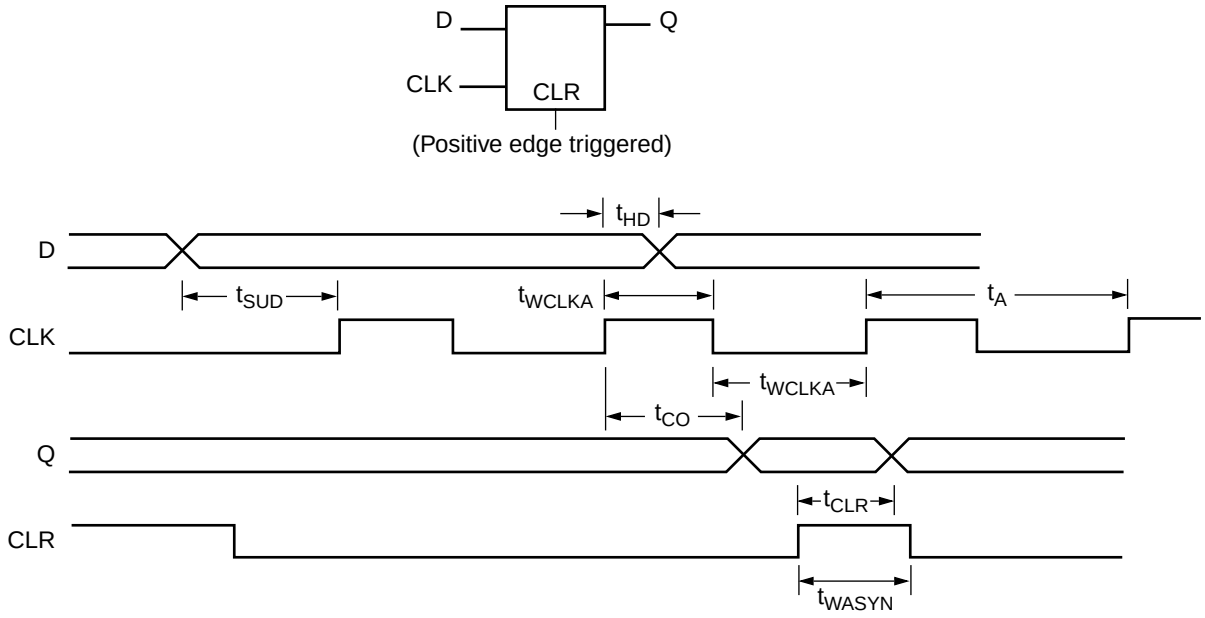


Module Delays

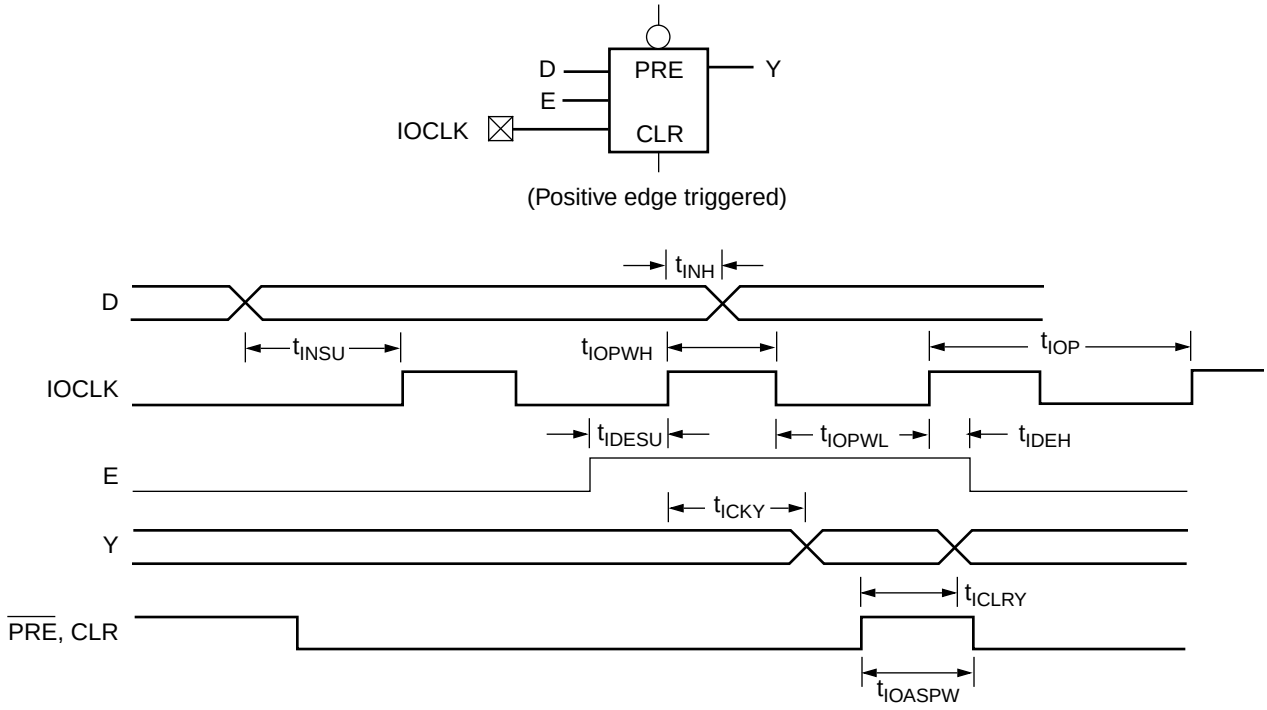


Sequential Module Timing Characteristics

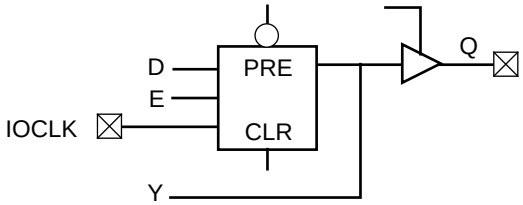
Flip-Flops



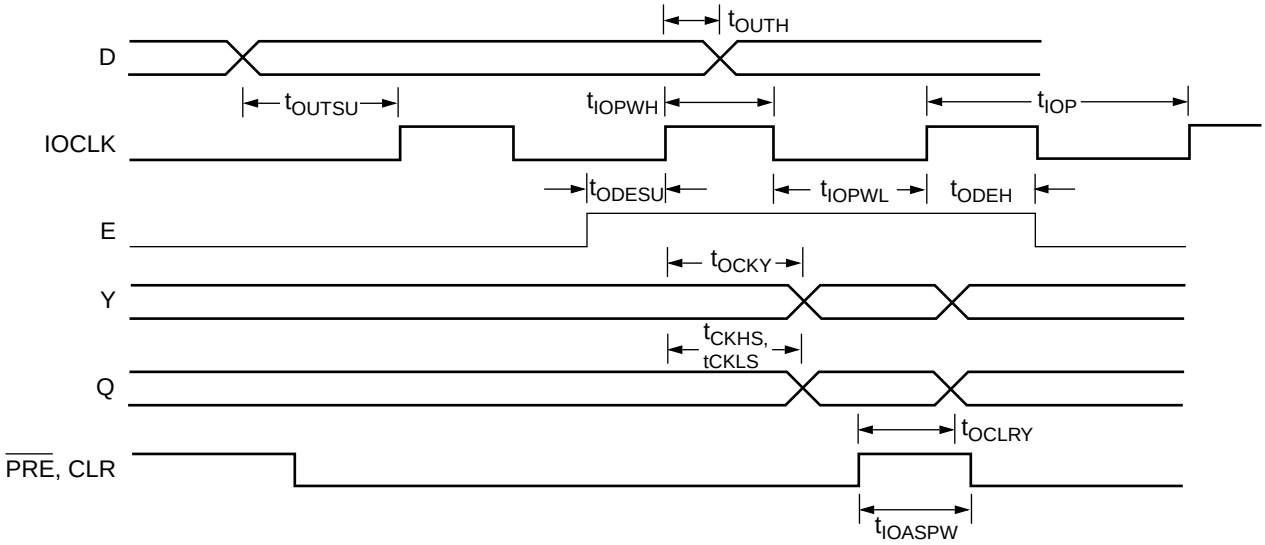
I/O Module: Sequential Input Timing Characteristics



I/O Module: Sequential Output Timing Characteristics



(Positive edge triggered)



Predictable Performance: Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track.

The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse.

The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

Table 2 • *Logic Module and Routing Delay by Fanout (ns) (Worst-Case Commercial Conditions)*

Speed	FO=1	FO=2	FO=3	FO=4	FO=8
ACT 3 –3	2.9	3.2	3.4	3.7	4.8

Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximatley 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	**Max.**	**Min.**	**Max.**
(Commercial Minimum/Maximum Specification) x	0.66	1.07	0.63	1.17

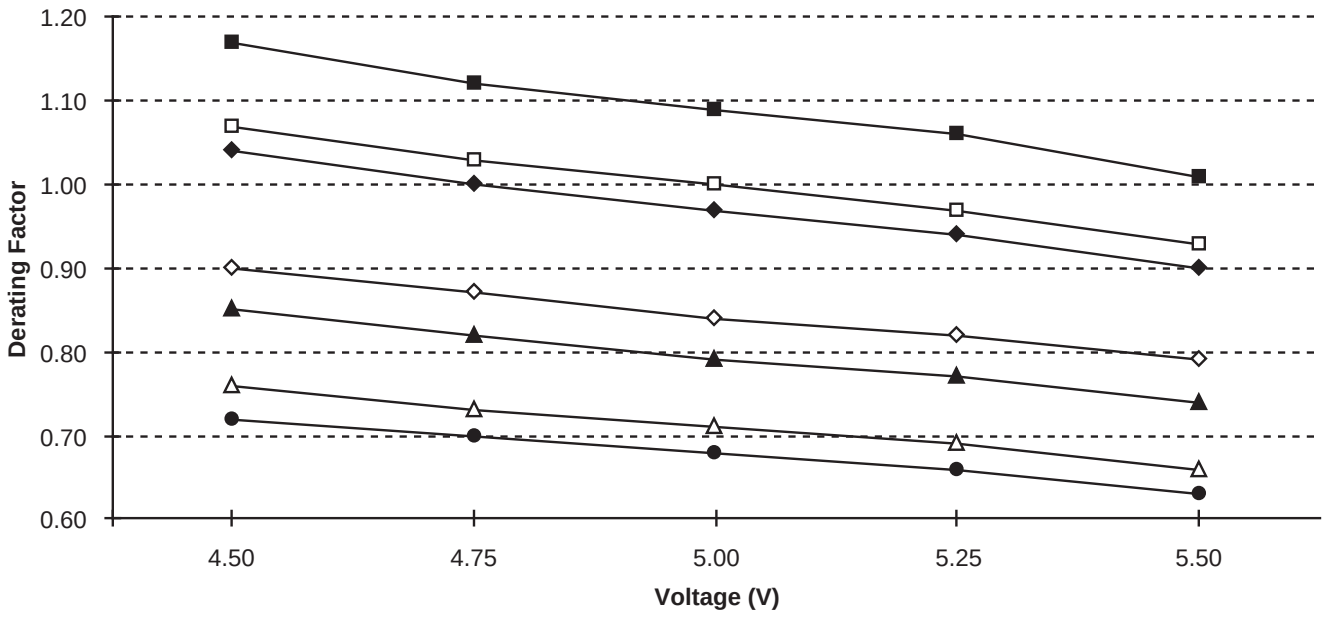
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	–55	**–40**	**0**	**25**	**70**	**85**	**125**
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.17
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01

Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)



Note: *This derating factor applies to all routing and propagation dealys.*

A1415A, A14V15A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		**'–3' Speed**		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**3.3V Speed[1]**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[3]												
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A, A14V15A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[1]												
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing												
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.0		2.3		2.5		3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.4		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	1.3		1.5		1.7		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A, A14V15A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		7.5		7.5		9.0		10.0		13.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		11.3		11.3		13.5		15.0		19.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		6.7		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		6.7		7.5		9.0		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		8.9		8.9		10.7		11.8		15.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		13.0		13.0		15.6		17.3		22.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

A1415A, A14V15A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IOPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network												
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO=64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO=64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO=128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO=64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO=64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0 0.0	1.0 3.0	ns

Note:

1. Delays based on 35pF loading.

A1425A, A14V25A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		**'–3' Speed**		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**3.3V Speed[1]**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[3]												
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1425A, A14V25A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[1]												
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing												
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	1.8		2.0		2.3		2.7		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.4		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	1.3		1.5		1.7		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1425A, A14V25A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		7.5		7.5		9.0		10.0		13.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		11.3		11.3		13.5		15.0		19.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		6.7		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		6.7		7.5		9.0		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		8.9		8.9		10.7		11.8		15.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		13.0		13.0		15.6		17.3		22.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

A1425A, A14V25A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IOPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network												
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO=64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO=64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO=128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO=64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO=64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
	(FO = 80)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 80)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

A1440A, A14V40A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		**'–3' Speed**		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**3.3V Speed[1]**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[3]												
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1440A, A14V40A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[1]												
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing												
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	1.5		1.7		2.0		2.3		2.3		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.4		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	1.3		1.5		1.7		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1440A, A14V40A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		8.5		8.5		9.5		11.0		14.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		11.3		11.3		13.5		15.0		19.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		9.0		9.0		10.1		11.8		14.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		13.0		13.0		15.6		17.3		22.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

A1440A, A14V40A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IOPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network												
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO=64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO=64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO=128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO=64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO=64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
	(FO = 144)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 144)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

A1460A, A14V60A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		**'–3' Speed**		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**3.3V Speed[1]**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[3]												
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A, A14V60A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[1]												
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing												
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	1.3		1.5		1.8		2.0		2.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.4		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	1.3		1.5		1.7		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A, A14V60A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		7.8		8.7		9.9		11.6		15.1	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		9.0		9.0		10.0		11.5		15.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		12.8		12.8		15.3		17.0		22.1	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.4		10.4		12.1		13.8		17.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		14.5		14.5		17.4		19.3		25.1	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

A1460A, A14V60A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.3		2.6		3.0		3.5		4.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t_{IOPWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.6		0.6		0.6	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (Hard-Wired) Array Clock Network												
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.6		0.6		0.6	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO=256)		6.0		6.8		7.7		9.0		11.8	ns
t_{RCKL}	Input High to Low (FO=256)		6.0		6.8		7.7		9.0		11.8	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	4.1		4.5		5.4		6.1		8.2		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	4.1		4.5		5.4		6.1		8.2		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.2		1.4		1.6		1.8		1.8	ns
t_{RP}	Minimum Period (FO=256)	8.3		9.3		11.1		12.5		16.7		ns
f_{RMAX}	Maximum Frequency (FO=256)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	0.0	5.0	ns
	(FO = 216)	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 216)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

A14100A, A14V100A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed[1]		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[3]												
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. *V_{CC} = 3.0 V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[1]												
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing												
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	1.2		1.4		1.5		1.8		1.8		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		1.0		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	0.7		0.8		1.0		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.5		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	1.3		1.5		2.0		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		9.5		9.5		10.5		12.0		15.6	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		12.8		12.8		15.3		17.0		22.1	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		8.0		9.0		10.0		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.4		10.4		12.4		13.8		17.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		14.5		14.5		17.4		19.3		25.1	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

A14100A, A14V100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

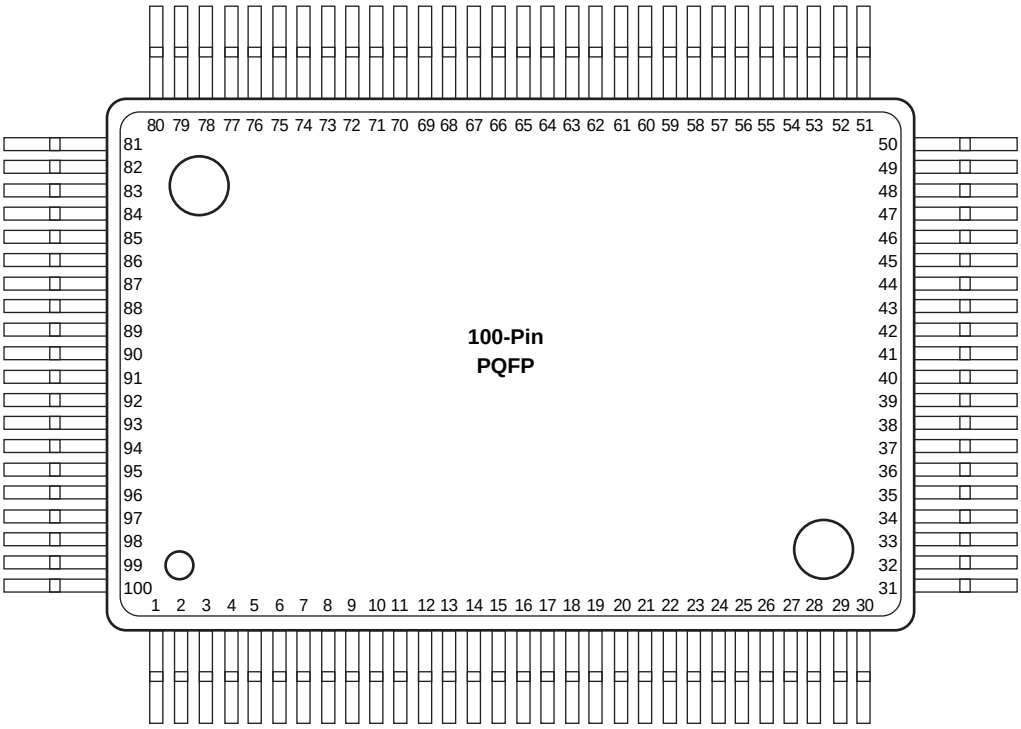
Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.3		2.6		3.0		3.5		4.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{IOPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (Hard-Wired) Array Clock Network												
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO=256)		6.0		6.8		7.7		9.0		11.8	ns
t_{RCKL}	Input High to Low (FO=256)		6.0		6.8		7.7		9.0		11.8	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	4.1		4.5		5.4		6.1		8.2		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	4.1		4.5		5.4		6.1		8.2		ns
t_{RCKSW}	Maximum Skew (FO=128)		1..2		1.4		1.6		1.8		1.8	ns
t_{RP}	Minimum Period (FO=256)	8.3		9.3		11.1		12.5		16.7		ns
f_{RMAX}	Maximum Frequency (FO=256)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	 0.0 0.0	 1.7 5.0	 0.0 0.0	 17 5.0	 0.0 0.0	 1.7 5.0	 0.0 0.0	 1.7 5.0	 0.0 0.0	 5.0 5.0	 ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	 0.0 0.0	 1.3 3.0	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	 ns

Note:

1. Delays based on 35pF loading.

Package Pin Assignments

100-Pin PQFP (Top View)



Pin Number	A1415 Function	A1425 Function
2	IOCLK, I/O	IOCLK, I/O
14	CLKA, I/O	CLKA, I/O
15	CLKB, I/O	CLKB, I/O
16	VCC	VCC
17	GND	GND
18	VCC	VCC
19	GND	GND
20	PRA, I/O	PRA, I/O
27	DCLK, I/O	DCLK, I/O
28	GND	GND
29	SDI, I/O	SDI, I/O
34	MODE	MODE
35	VCC	VCC
36	GND	GND
47	GND	GND

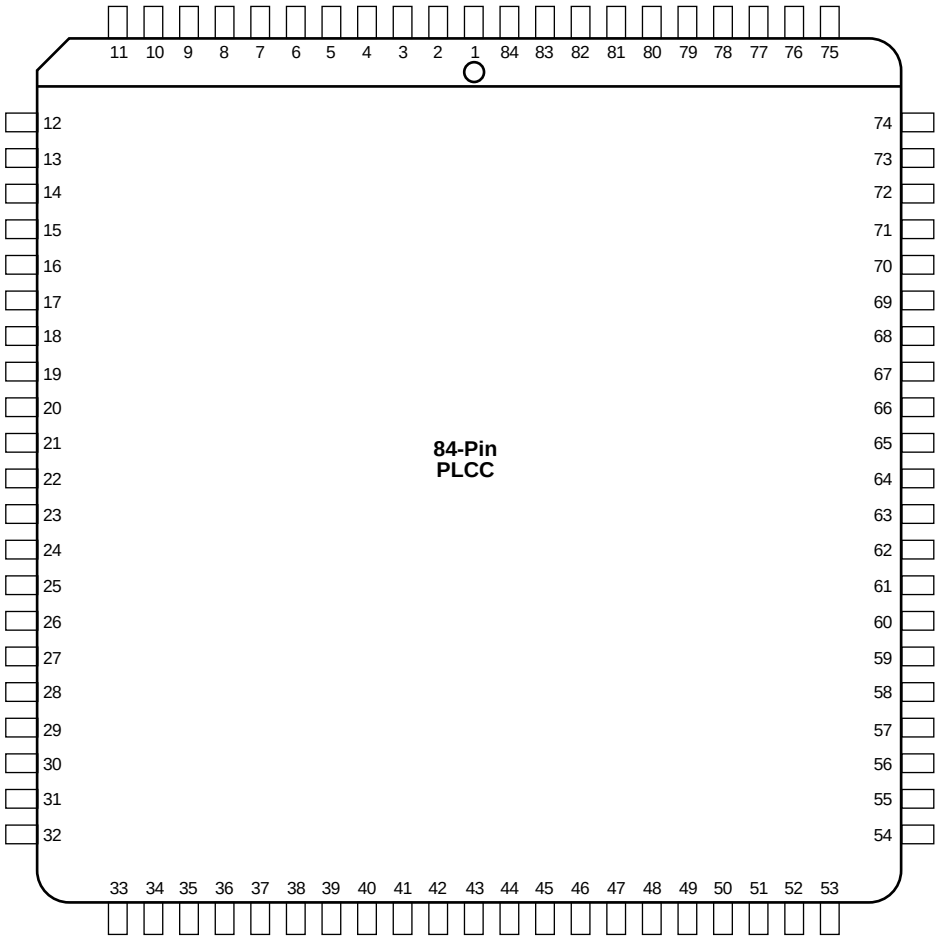
Pin Number	A1415 Function	A1425 Function
48	VCC	VCC
61	PRB, I/O	PRB, I/O
62	GND	GND
63	VCC	VCC
64	GND	GND
65	VCC	VCC
67	HCLK, I/O	HCLK, I/O
78	IOPCL, I/O	IOPCL, I/O
79	GND	GND
85	VCC	VCC
86	VCC	VCC
87	GND	GND
96	VCC	VCC
97	GND	GND

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin PLCC (Top View)



84-Pin PLCC

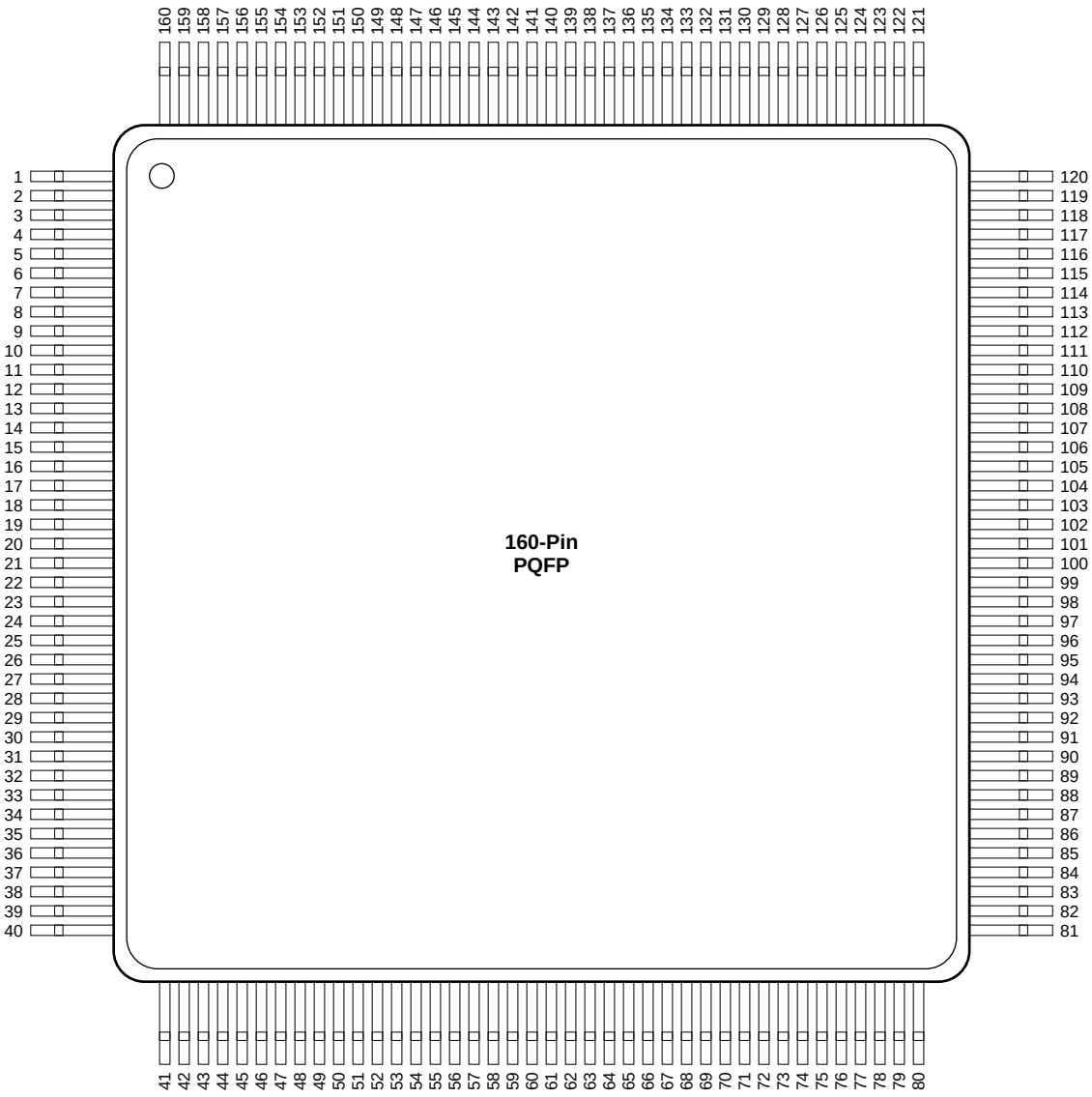
Pin Number	A1415 A14V15 Function	A1425 A14V25 Function	A1440 A14V40 Function
1	VCC	VCC	VCC
2	GND	GND	GND
3	VCC	VCC	VCC
4	PRA, I/O	PRA, I/O	PRA, I/O
11	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	SDI, I/O	SDI, I/O	SDI, I/O
16	MODE	MODE	MODE
27	GND	GND	GND
28	VCC	VCC	VCC
40	PRB, I/O	PRB, I/O	PRB, I/O
41	VCC	VCC	VCC
42	GND	GND	GND
43	VCC	VCC	VCC
45	HCLK, I/O	HCLK, I/O	HCLK, I/O
53	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
59	VCC	VCC	VCC
60	VCC	VCC	VCC
61	GND	GND	GND
68	VCC	VCC	VCC
69	GND	GND	GND
74	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	CLKB, I/O	CLKB, I/O	CLKB, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

160-Pin PQFP (Top View)



160-Pin PQFP

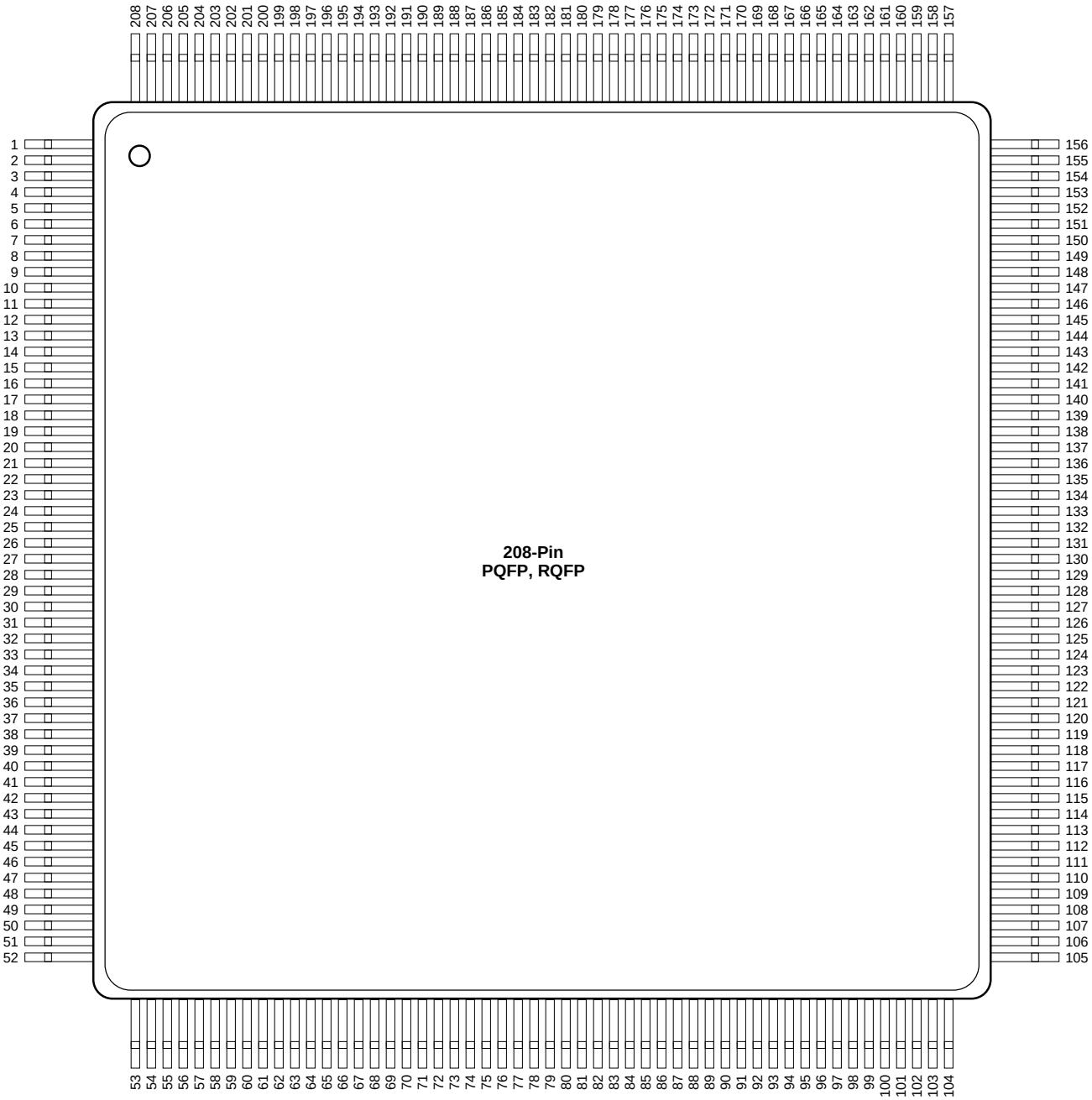
Pin Number	A1425 A14V25 Function	A1440 A14V40 Function	A1460 A14V60 Function
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

208-Pin PQFP, RQFP (Top View)



208-Pin PQFP, RQFP

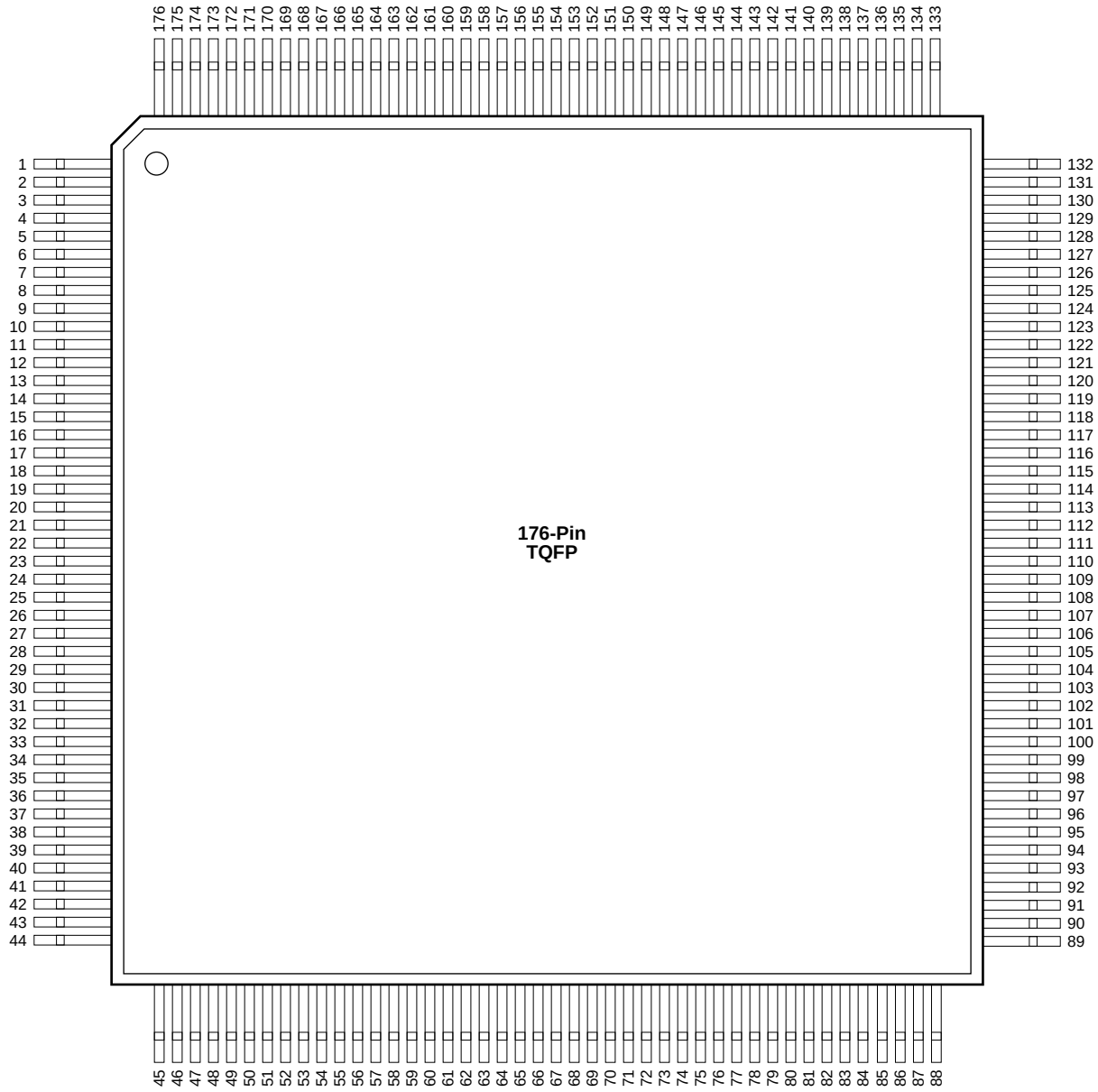
Pin Number	A1460 A14V60 Function	A14100 A14V100 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	VCC	VCC
25	VCC	VCC
26	GND	GND
27	VCC	VCC
28	GND	GND
40	VCC	VCC
41	VCC	VCC
52	GND	GND
53	NC	I/O
60	VCC	VCC
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	VCC	VCC
79	GND	GND
80	VCC	VCC
82	HCLK, I/O	HCLK, I/O
98	VCC	VCC
102	NC	I/O
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	VCC	VCC
115	VCC	VCC
116	NC	I/O
129	GND	GND
130	VCC	VCC
131	GND	GND
132	VCC	VCC
145	VCC	VCC
146	GND	GND
147	NC	I/O
148	VCC	VCC
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	VCC	VCC
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	VCC	VCC
183	GND	GND
184	VCC	VCC
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	VCC	VCC
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

176-Pin TQFP (Top View)



176-Pin TQFP

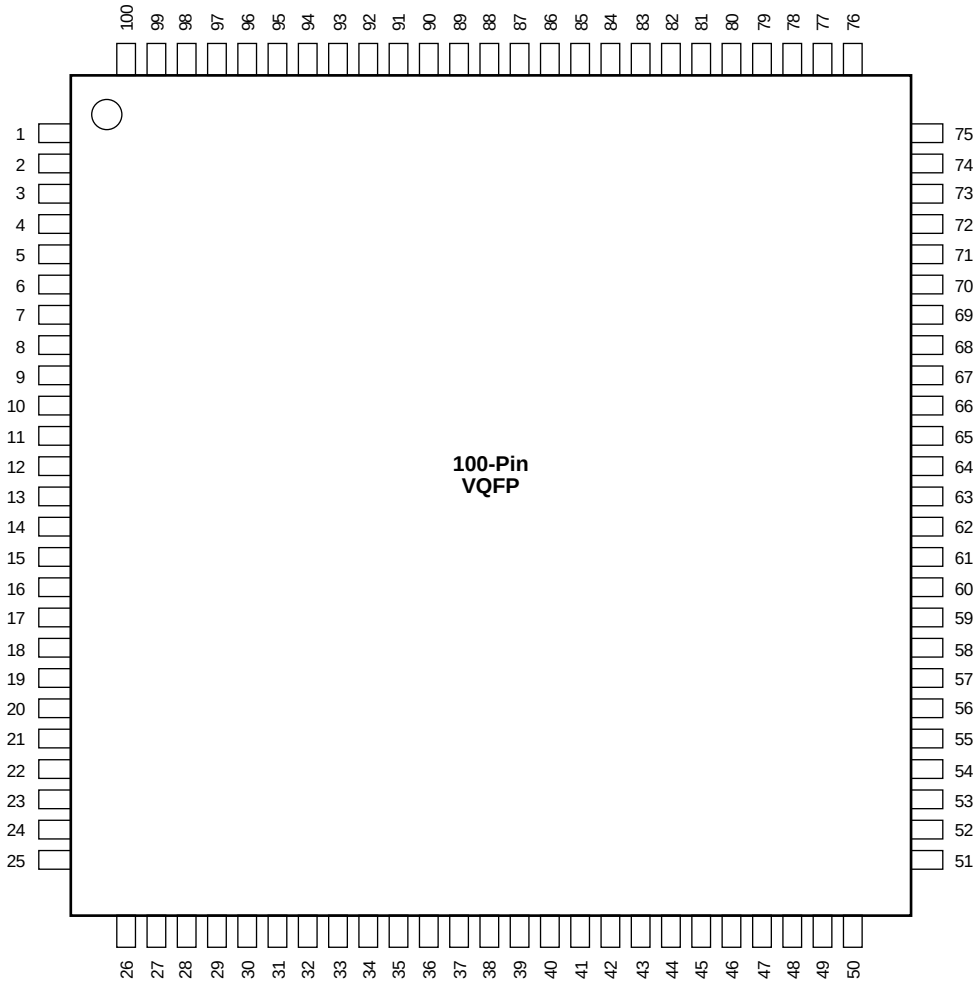
Pin Number	A1440 A14V40 Function	A1460 A14V60 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
10	MODE	MODE
11	VCC	VCC
20	NC	I/O
21	GND	GND
22	VCC	VCC
23	GND	GND
32	VCC	VCC
33	VCC	VCC
44	GND	GND
49	NC	I/O
51	NC	I/O
63	NC	I/O
64	PRB, I/O	PRB, I/O
65	GND	GND
66	VCC	VCC
67	VCC	VCC
69	HCLK, I/O	HCLK, I/O
82	NC	I/O
83	NC	I/O
88	IOPCL, I/O	IOPCL, I/O
89	GND	GND
98	VCC	VCC
99	VCC	VCC
108	GND	GND
109	VCC	VCC
110	GND	GND
119	NC	I/O
121	NC	I/O
122	VCC	VCC
123	GND	GND
124	VCC	VCC
132	IOCLK, I/O	IOCLK, I/O
133	GND	GND
138	NC	I/O
152	CLKA, I/O	CLKA, I/O
153	CLKB, I/O	CLKB, I/O
154	VCC	VCC
155	GND	GND
156	VCC	VCC
157	PRA, I/O	PRA, I/O
158	NC	I/O
170	NC	I/O
176	DCLK, I/O	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin VQFP (Top View)



100-Pin VQFP

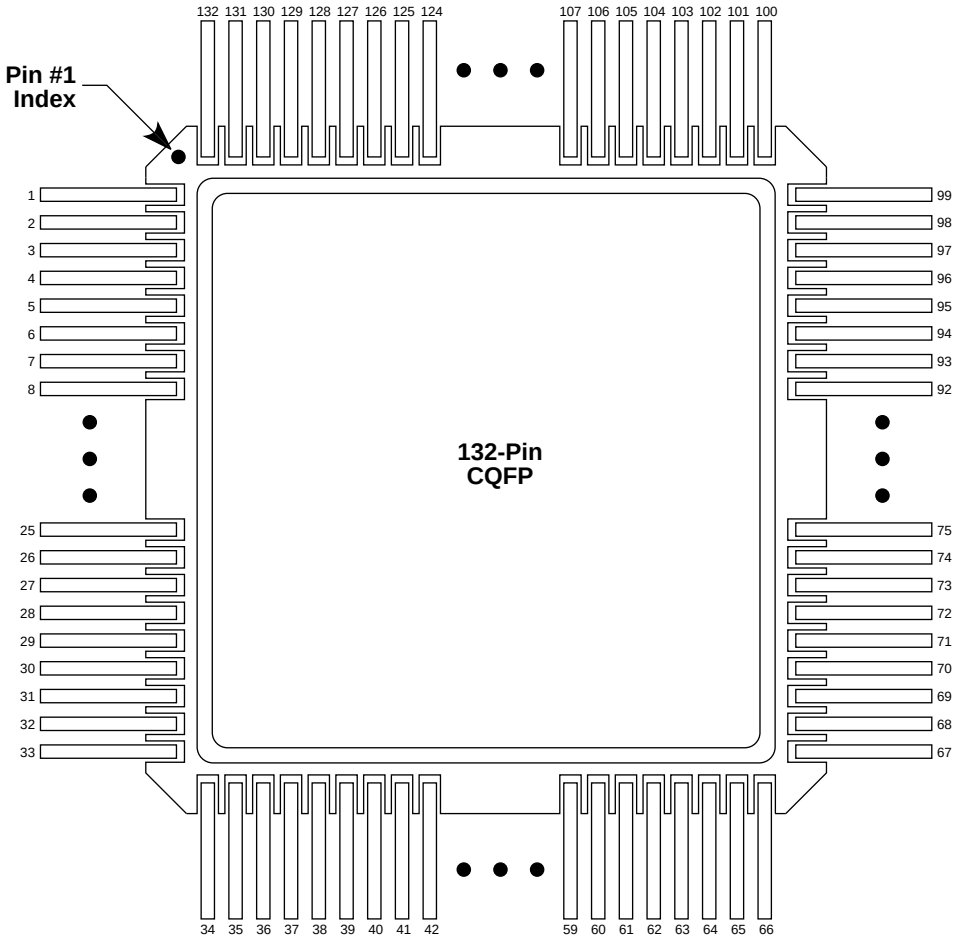
Pin Number	A1415 A14V15 Function	A1425 A14V25 Function	A1440 A14V40 Function
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
7	MODE	MODE	MODE
8	VCC	VCC	VCC
9	GND	GND	GND
20	VCC	VCC	VCC
21	NC	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCC	VCC	VCC
36	GND	GND	GND
37	VCC	VCC	VCC
39	HCLK, I/O	HCLK, I/O	HCLK, I/O
50	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
51	GND	GND	GND
57	VCC	VCC	VCC
58	VCC	VCC	VCC
67	VCC	VCC	VCC
68	GND	GND	GND
69	GND	GND	GND
74	NC	I/O	I/O
75	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
87	CLKA, I/O	CLKA, I/O	CLKA, I/O
88	CLKB, I/O	CLKB, I/O	CLKB, I/O
89	VCC	VCC	VCC
90	VCC	VCC	VCC
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	NC	I/O	I/O
100	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assigments (continued)

132-Pin CQFP (Top View)



132-Pin CQFP

Pin Number	A1425 Function
1	NC
2	GND
3	SDI, I/O
9	MODE
10	GND
11	VCC
22	VCC
26	GND
27	VCC
34	NC
36	GND
42	GND
43	VCC
48	PRB, I/O
50	HCLK, I/O
58	GND
59	VCC
64	IOPCL, I/O
65	GND
66	NC
67	NC

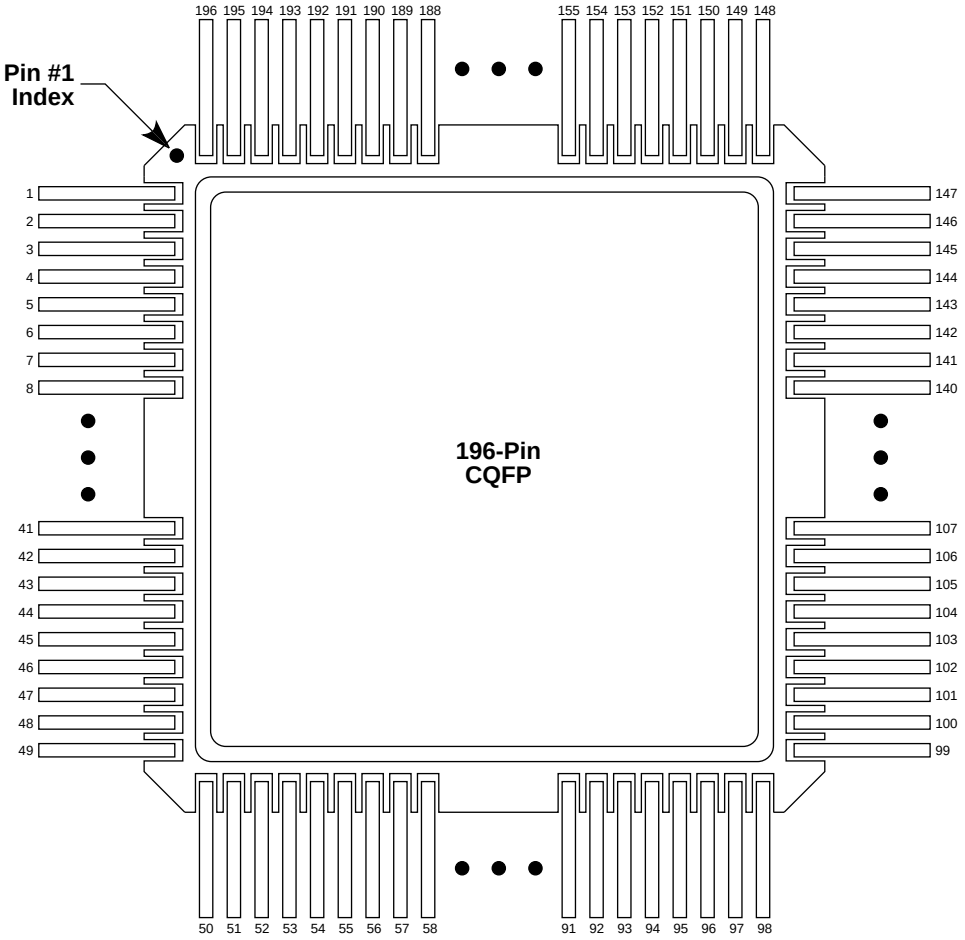
Pin Number	A1425 Function
74	GND
75	VCC
78	VCC
89	VCC
90	GND
91	VCC
92	GND
98	IOCLK, I/O
99	NC
100	NC
101	GND
106	GND
107	VCC
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
122	GND
123	VCC
131	DCLK, I/O
132	NC

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assigments (continued)

196-Pin CQFP (Top View)



196-Pin CQFP

Pin Number	A1460 Function
1	GND
2	SDI, I/O
11	MODE
12	VCC
13	GND
37	GND
38	VCC
39	VCC
51	GND
52	GND
59	VCC
64	GND
77	HCLK, I/O
79	PRB, I/O
86	GND
94	VCC
98	GND
100	IOPCL, I/O
101	GND

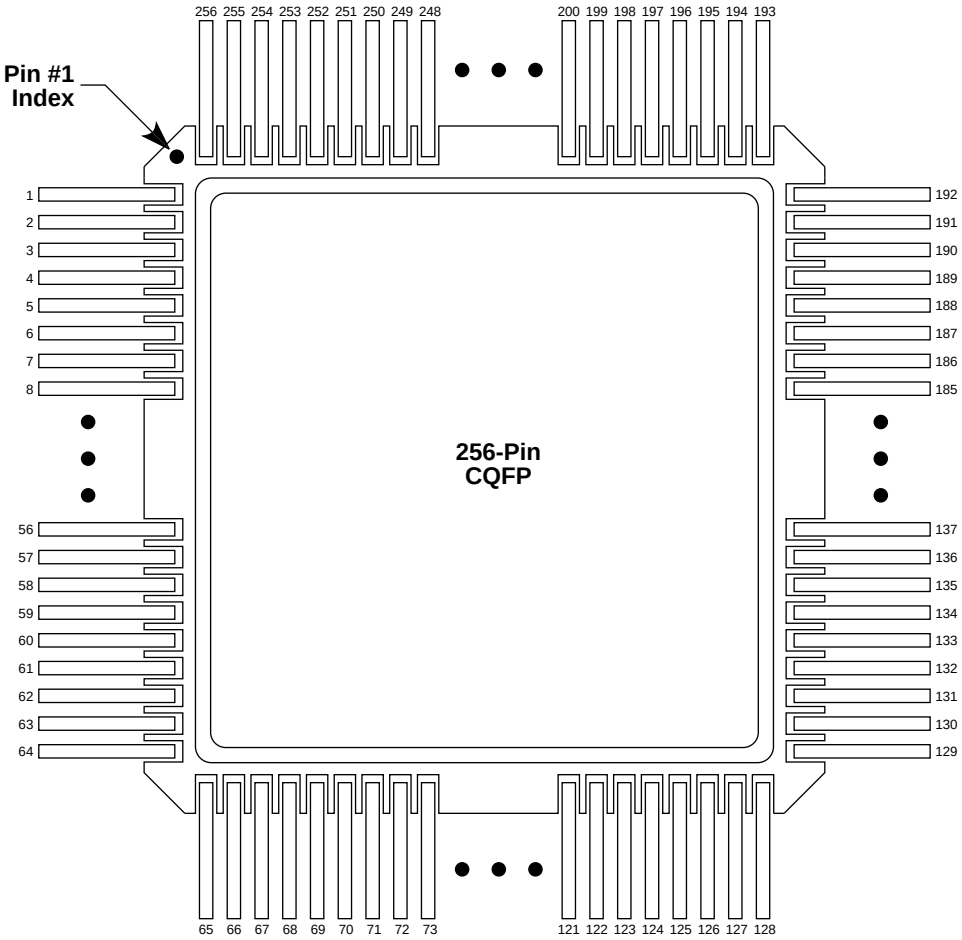
Pin Number	A1460 Function
110	VCC
111	VCC
112	GND
137	VCC
138	GND
139	GND
140	VCC
148	IOCLK, I/O
149	GND
155	VCC
162	GND
172	CLKA, I/O
173	CLKB, I/O
174	PRA, I/O
183	GND
189	VCC
193	GND
196	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC : Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assigments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	A14100 Function
1	GND
2	SDI, I/O
11	MODE
28	VCC
29	GND
30	VCC
31	GND
46	VCC
59	GND
90	PRB, I/O
91	GND
92	VCC
93	GND
94	VCC
96	HCLK, I/O
110	GND
127	IOPCL, I/O
128	GND
141	VCC

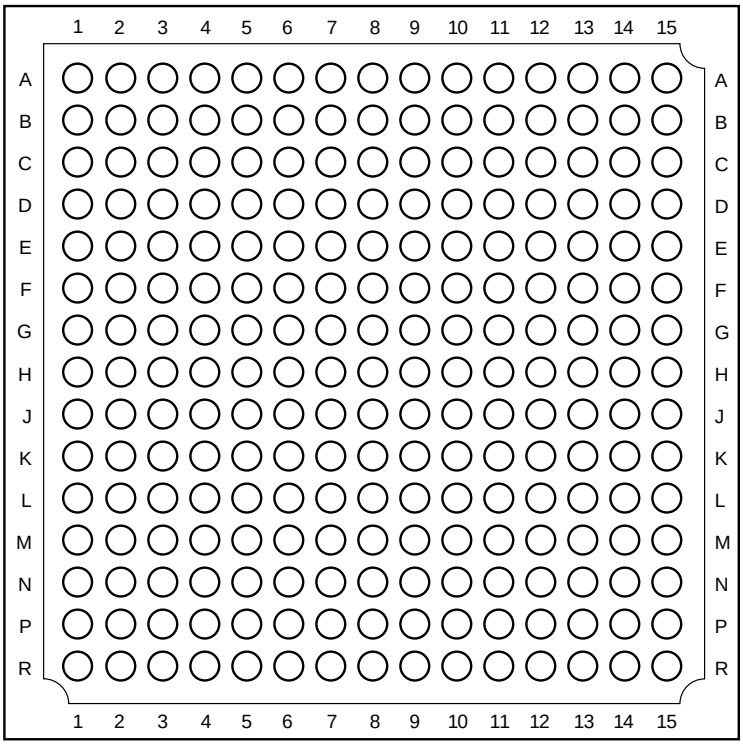
Pin Number	A14100 Function
158	GND
159	VCC
160	GND
161	VCC
174	VCC
175	GND
176	GND
188	IOCLK, I/O
189	GND
219	CLKA, I/O
220	CLKB, I/O
221	VCC
222	GND
223	VCC
224	GND
225	PRA, I/O
240	GND
256	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes No Connection*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

225-Pin BGA (Top View)



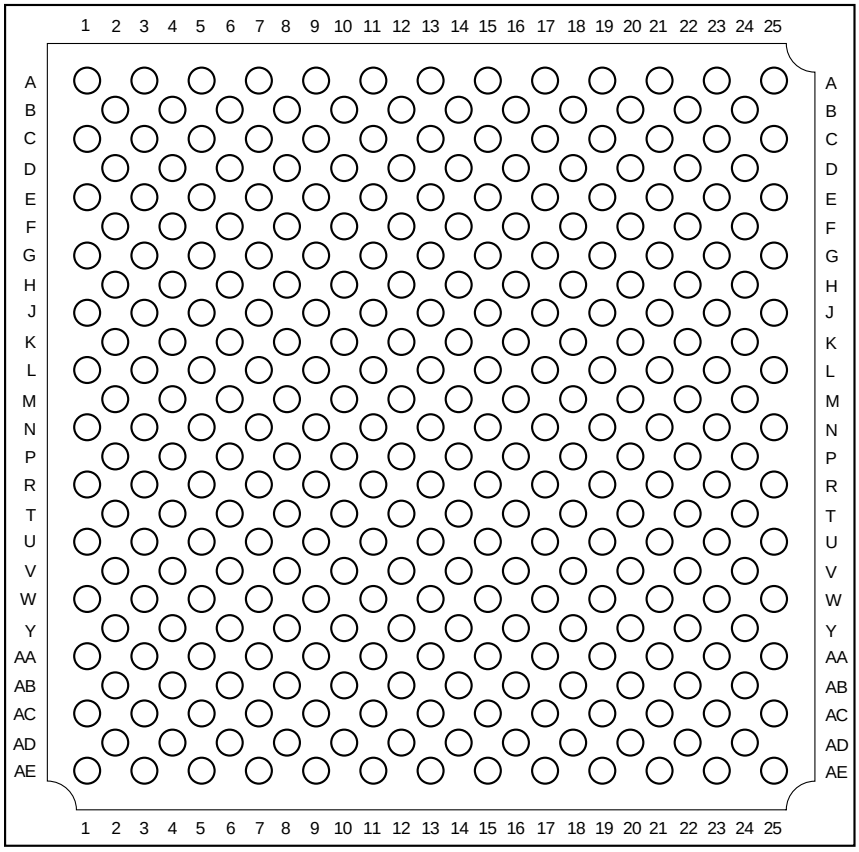
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA OR I/O	A7
PRB or I/O	L7
SDI or I/O	D4
V_{CC}	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

313-Pin BGA (Top View)



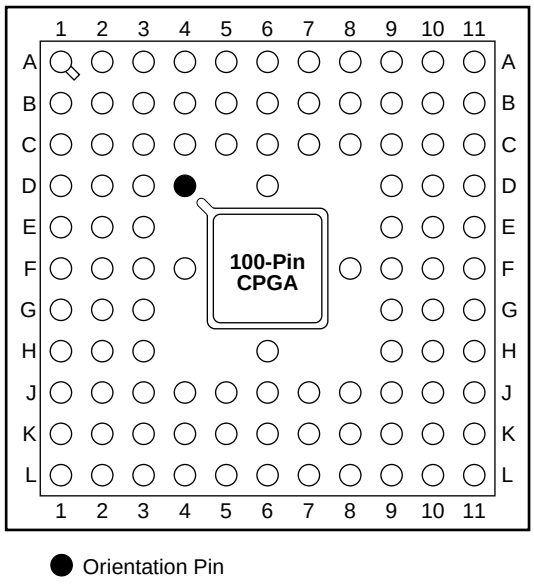
A14100 A14V100 Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA OR I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
V_{CC}	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin CPGA (Top View)



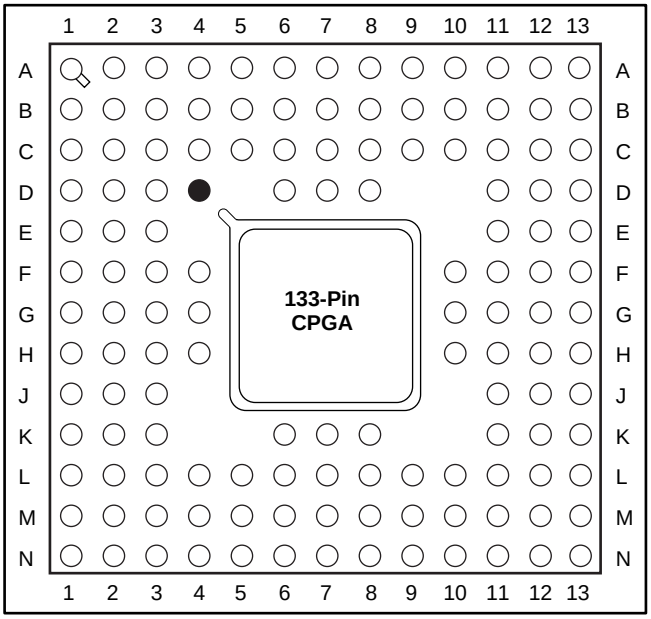
A1415 Function	Location
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA OR I/O	A6
PRB or I/O	L3
SDI or I/O	B3
V_{CC}	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

133-Pin CPGA (Top View)



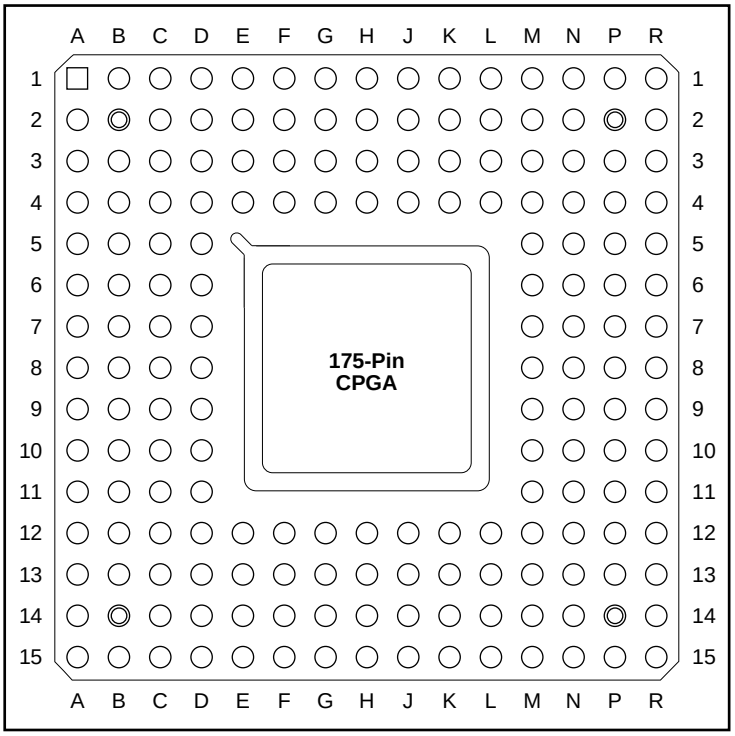
A1425 Function	Location
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA OR I/O	A6
PRB or I/O	L6
SDI or I/O	C2
V_{CC}	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

175-Pin CPGA (Top View)



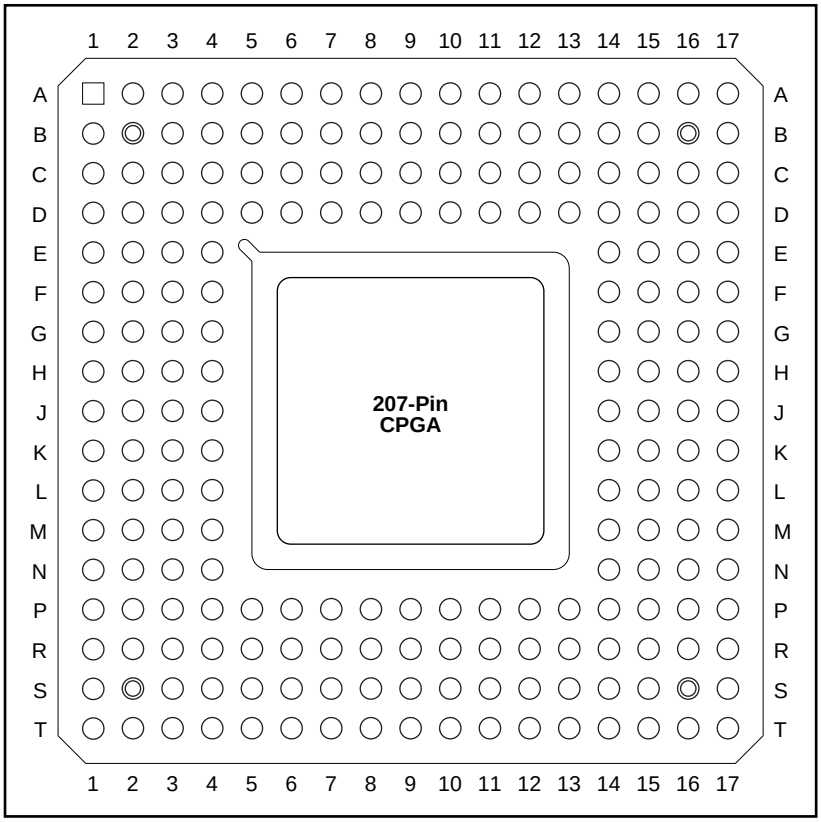
A1440 Function	Location
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA OR I/O	B8
PRB or I/O	R7
SDI or I/O	D3
V_{CC}	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

207-Pin CPGA (Top View)



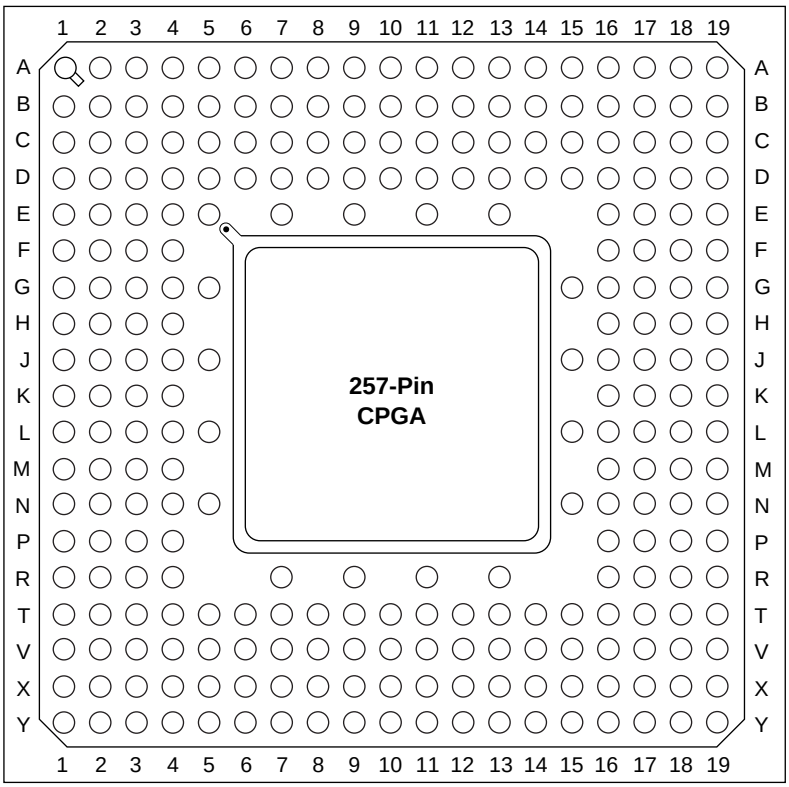
A1460 Function	Location
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C15, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15
HCKL or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA OR I/O	H1
PRB or I/O	K16
SDI or I/O	C3
V_{CC}	B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

257-Pin CPGA (Top View)



A14100 Function	Location
CLKA or I/O	L4
CLKB or I/O	L5
DCLK or I/O	E4
GND	B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7
HCLK or I/O	J16
IOCLK or I/O	T5
IOPCL or I/O	R16
MODE	A5
NC	E5
PRA OR I/O	J1
PRB or I/O	J17
SDI or I/O	B4
V_{CC}	C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*